FIG. 1
PRIOR ART

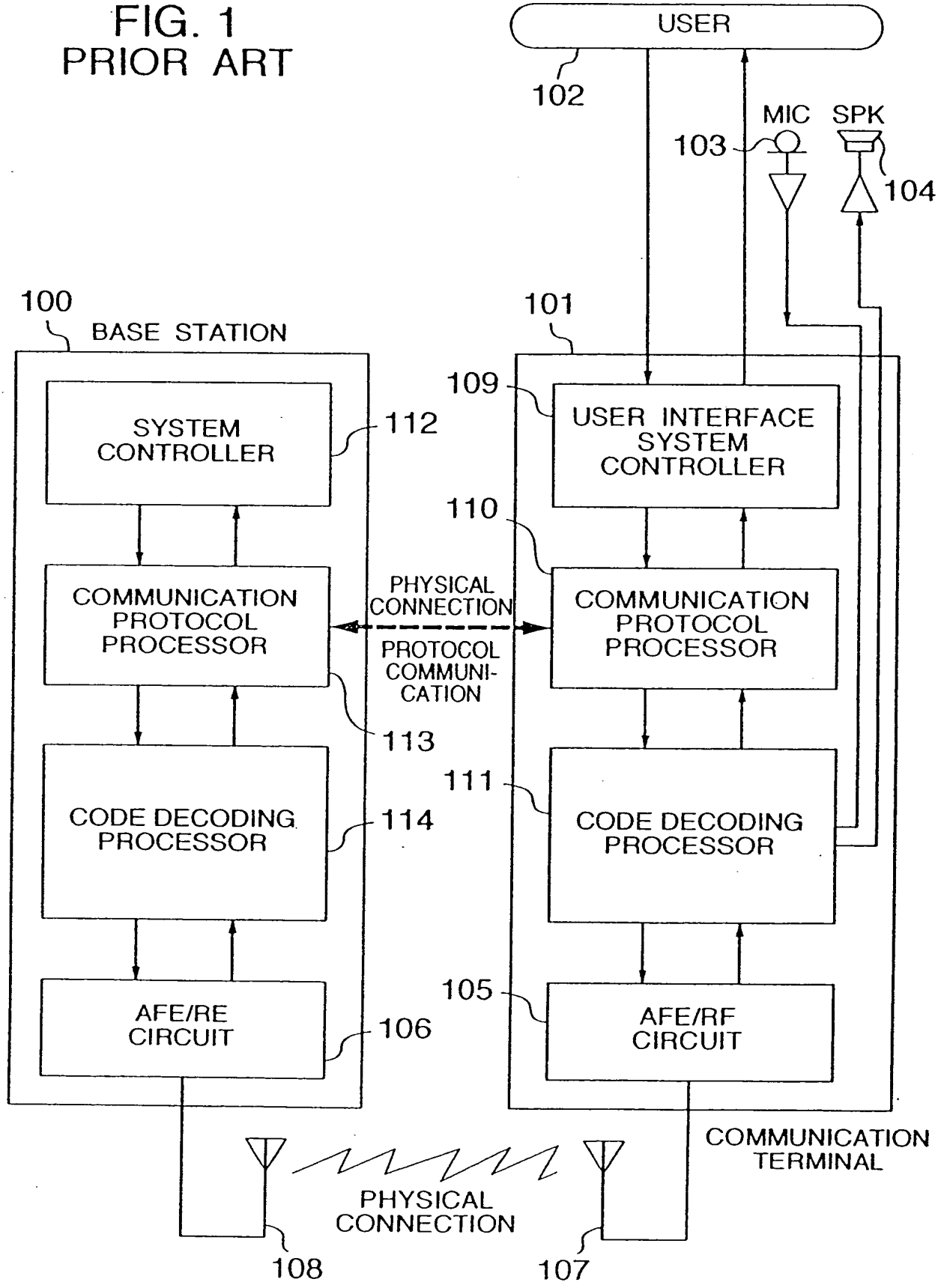


FIG. 2

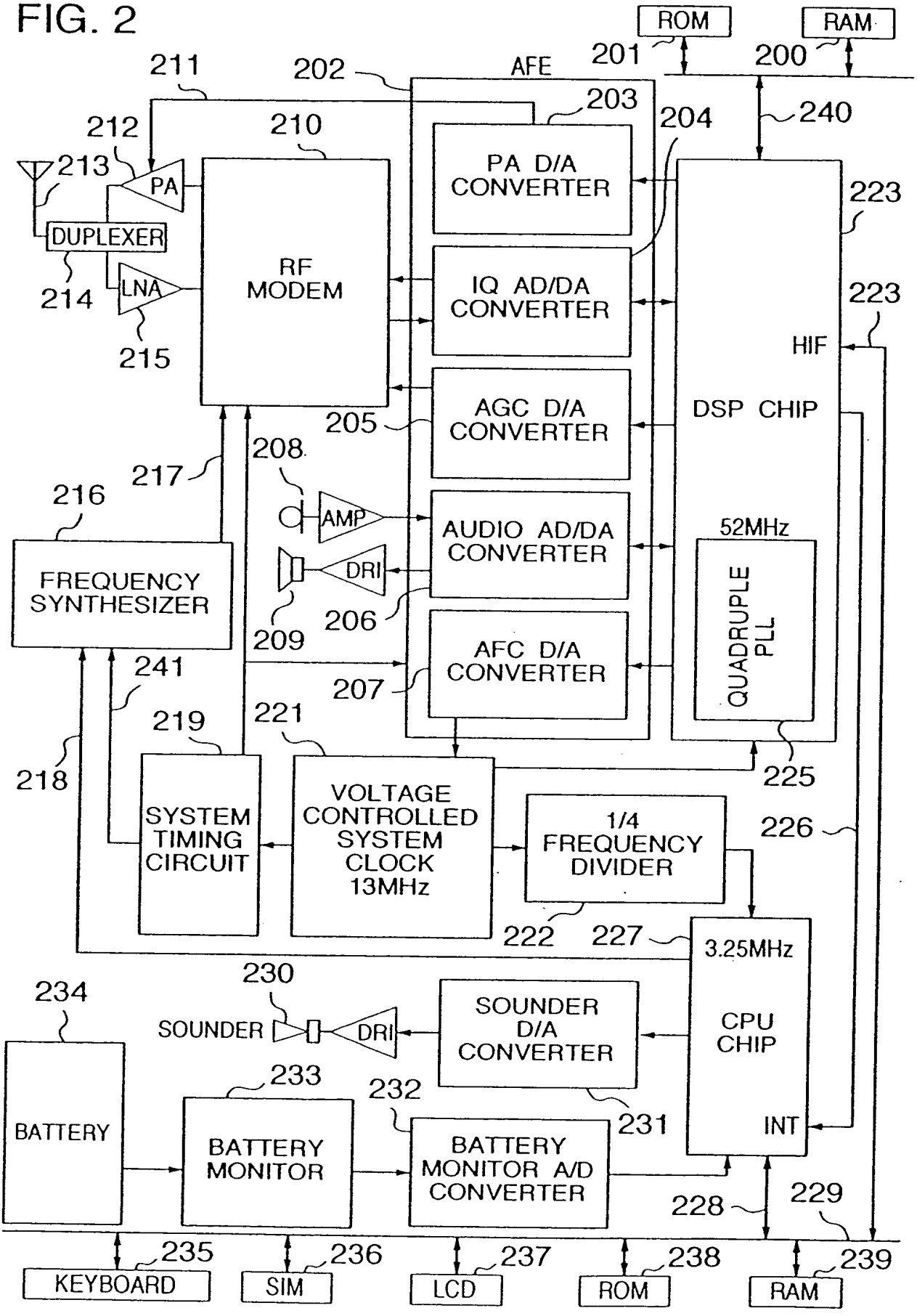

ROM
RAM
201
200
AFE
202
203
204
240
211
212
210
213
PA
PA D/A CONVERTER
223
DUPLEXER
214
LNA
RF MODEM
IQ AD/DA CONVERTER
223
215
HIF
AGC D/A CONVERTER
205
DSP CHIP
208
217
216
AMP
AUDIO AD/DA CONVERTER
52MHz
FREQUENCY SYNTHESIZER
DRI
QUADRUPLE PLL
209
206
AFC D/A CONVERTER
241
207
219
221
218
225
SYSTEM TIMING CIRCUIT
VOLTAGE CONTROLLED SYSTEM CLOCK 13MHz
1/4 FREQUENCY DIVIDER
226
222
227
3.25MHz
230
234
SOUNDER
DRI
SOUNDER D/A CONVERTER
CPU CHIP
233
232
BATTERY
BATTERY MONITOR
BATTERY MONITOR A/D CONVERTER
231
INT
228
229
235
236
237
238
239
KEYBOARD
SIM
LCD
ROM
RAM

FIG. 3

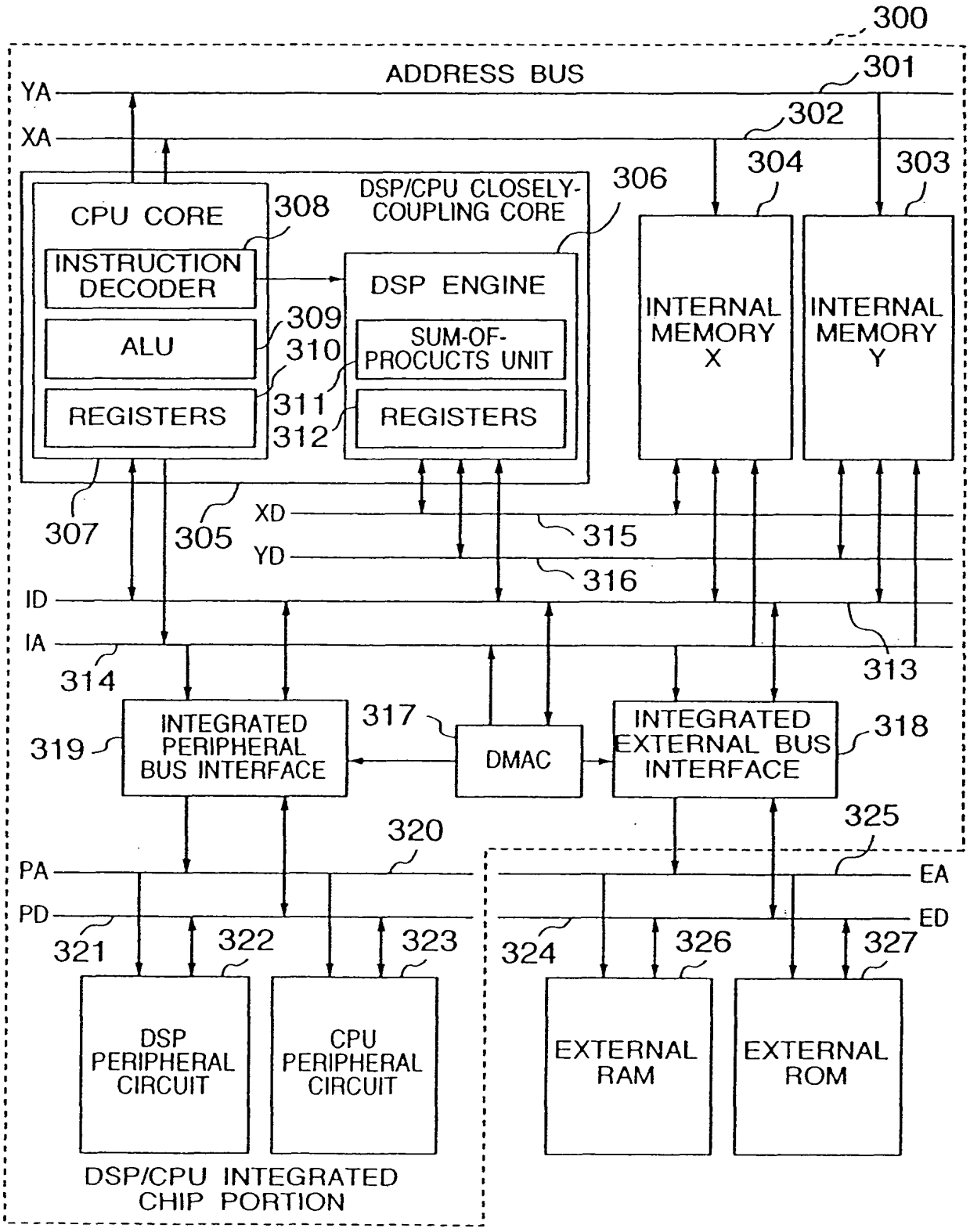

300
ADDRESS BUS
301
YA
302
XA
304
303
306
DSP/CPU CLOSELY-COUPLING CORE
CPU CORE
308
INSTRUCTION DECODER
ALU
309
310
REGISTERS
311
312
DSP ENGINE
SUM-OF-PROCUCTS UNIT
REGISTERS
INTERNAL MEMORY X
INTERNAL MEMORY Y
307
305
XD
315
YD
316
ID
IA
314
313
INTEGRATED PERIPHERAL BUS INTERFACE
319
317
DMAC
INTEGRATED EXTERNAL BUS INTERFACE
318
320
325
PA
EA
PD
ED
321
322
323
324
326
327
DSP PERIPHERAL CIRCUIT
CPU PERIPHERAL CIRCUIT
EXTERNAL RAM
EXTERNAL ROM
DSP/CPU INTEGRATED CHIP PORTION

FIG. 4

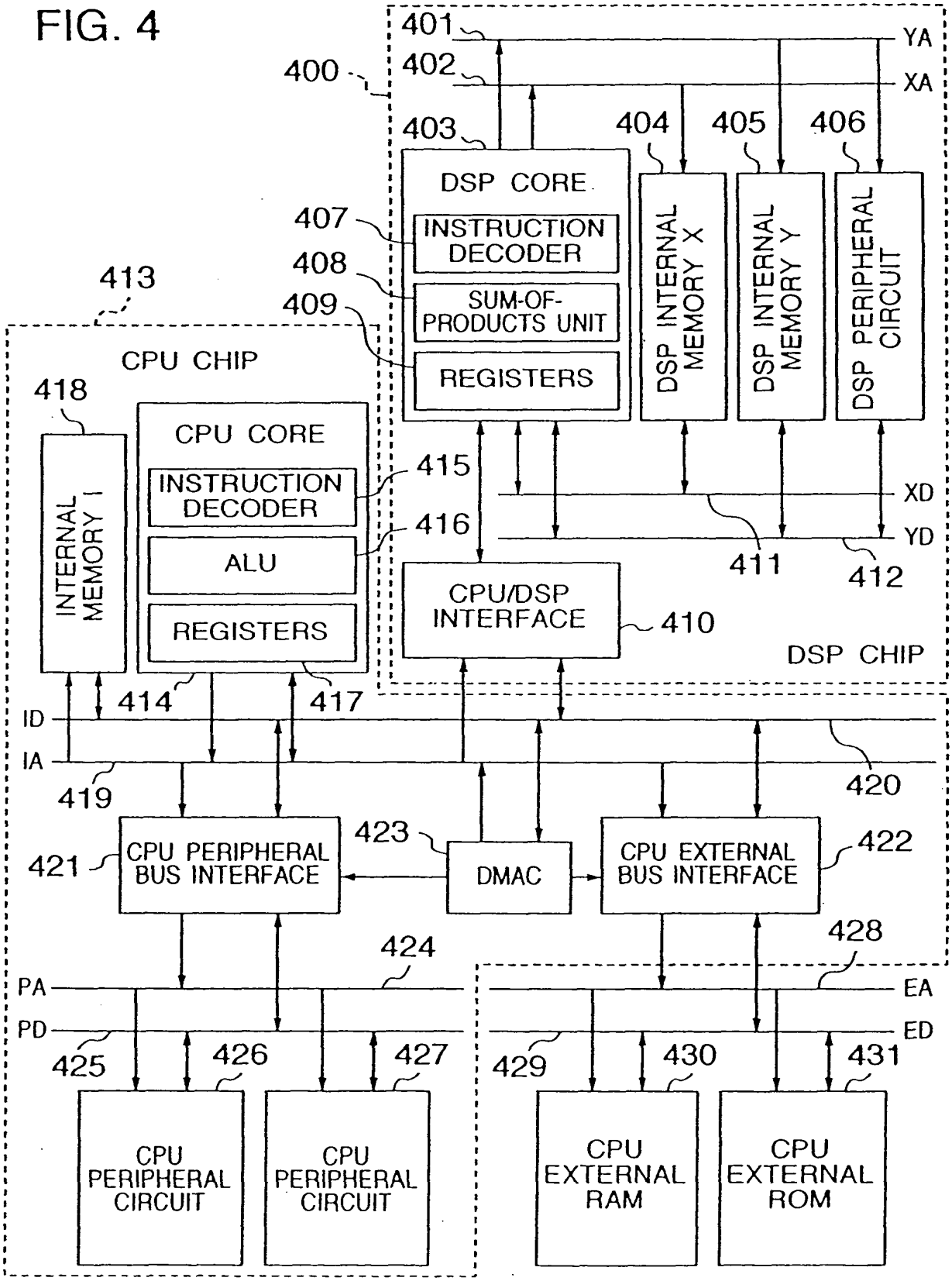

401
YA
402
XA
400
403
404
405
406
DSP CORE
INSTRUCTION DECODER
SUM-OF-PRODUCTS UNIT
REGISTERS
DSP INTERNAL MEMORY X
DSP INTERNAL MEMORY Y
DSP PERIPHERAL CIRCUIT
407
408
409
413
CPU CHIP
418
CPU CORE
INSTRUCTION DECODER
ALU
REGISTERS
INTERNAL MEMORY I
415
416
XD
YD
411
412
CPU/DSP INTERFACE
410
DSP CHIP
414
417
ID
IA
419
420
421
CPU PERIPHERAL BUS INTERFACE
423
DMAC
CPU EXTERNAL BUS INTERFACE
422
424
428
PA
EA
PD
ED
425
426
427
429
430
431
CPU PERIPHERAL CIRCUIT
CPU PERIPHERAL CIRCUIT
CPU EXTERNAL RAM
CPU EXTERNAL ROM

FIG. 5

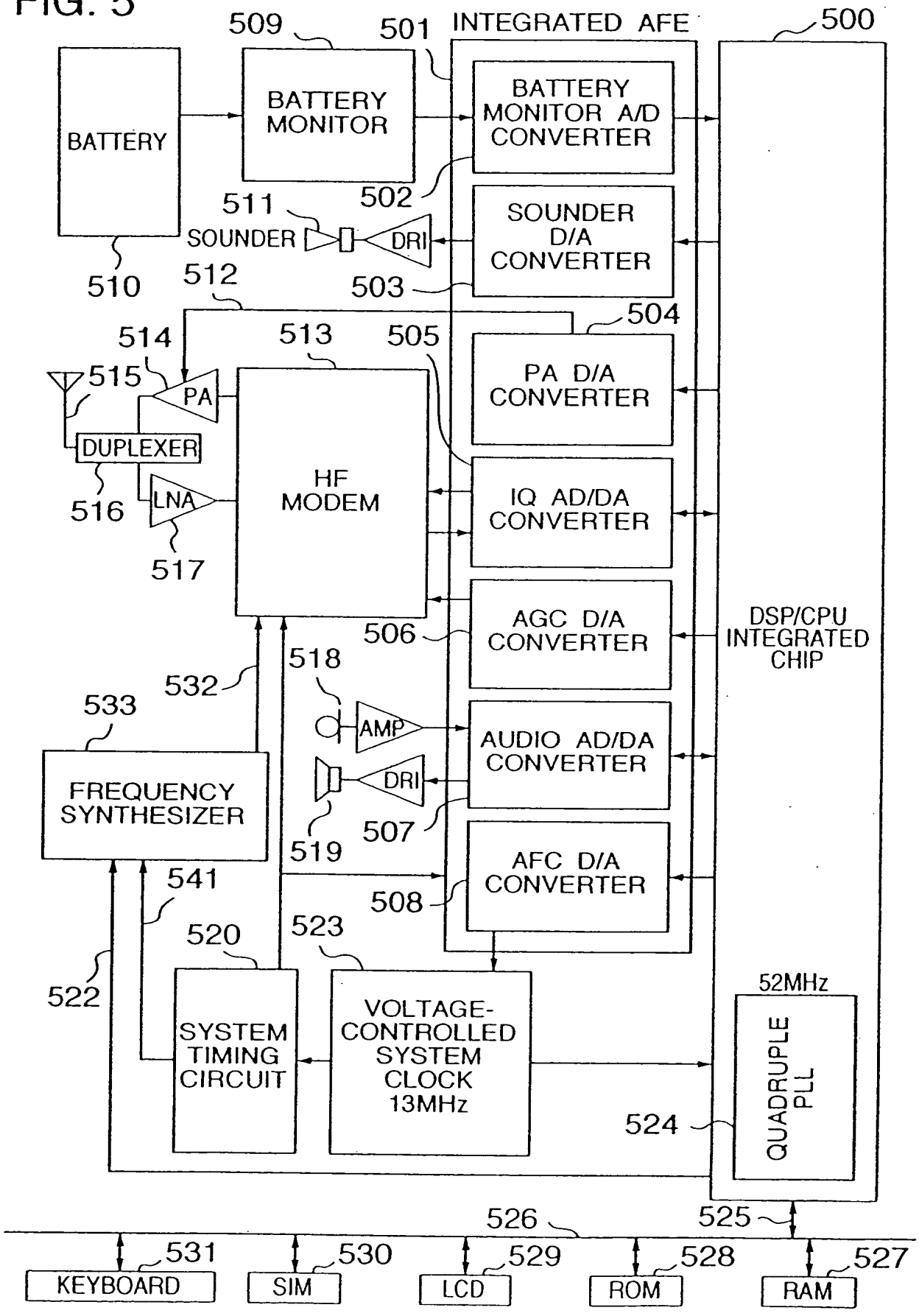

INTEGRATED AFE
500
509
501
BATTERY
BATTERY MONITOR
BATTERY MONITOR A/D CONVERTER
502
511
SOUNDER
DRI
SOUNDER D/A CONVERTER
503
510
512
504
514
513
505
515
PA
PA D/A CONVERTER
DUPLEXER
HF MODEM
IQ AD/DA CONVERTER
516
LNA
517
AGC D/A CONVERTER
506
DSP/CPU INTEGRATED CHIP
518
532
533
AMP
AUDIO AD/DA CONVERTER
FREQUENCY SYNTHESIZER
DRI
519
507
AFC D/A CONVERTER
508
541
520
523
522
52MHz
SYSTEM TIMING CIRCUIT
VOLTAGE-CONTROLLED SYSTEM CLOCK 13MHz
QUADRUPLE PLL
524
526
525
531
530
529
528
527
KEYBOARD
SIM
LCD
ROM
RAM

FIG. 6

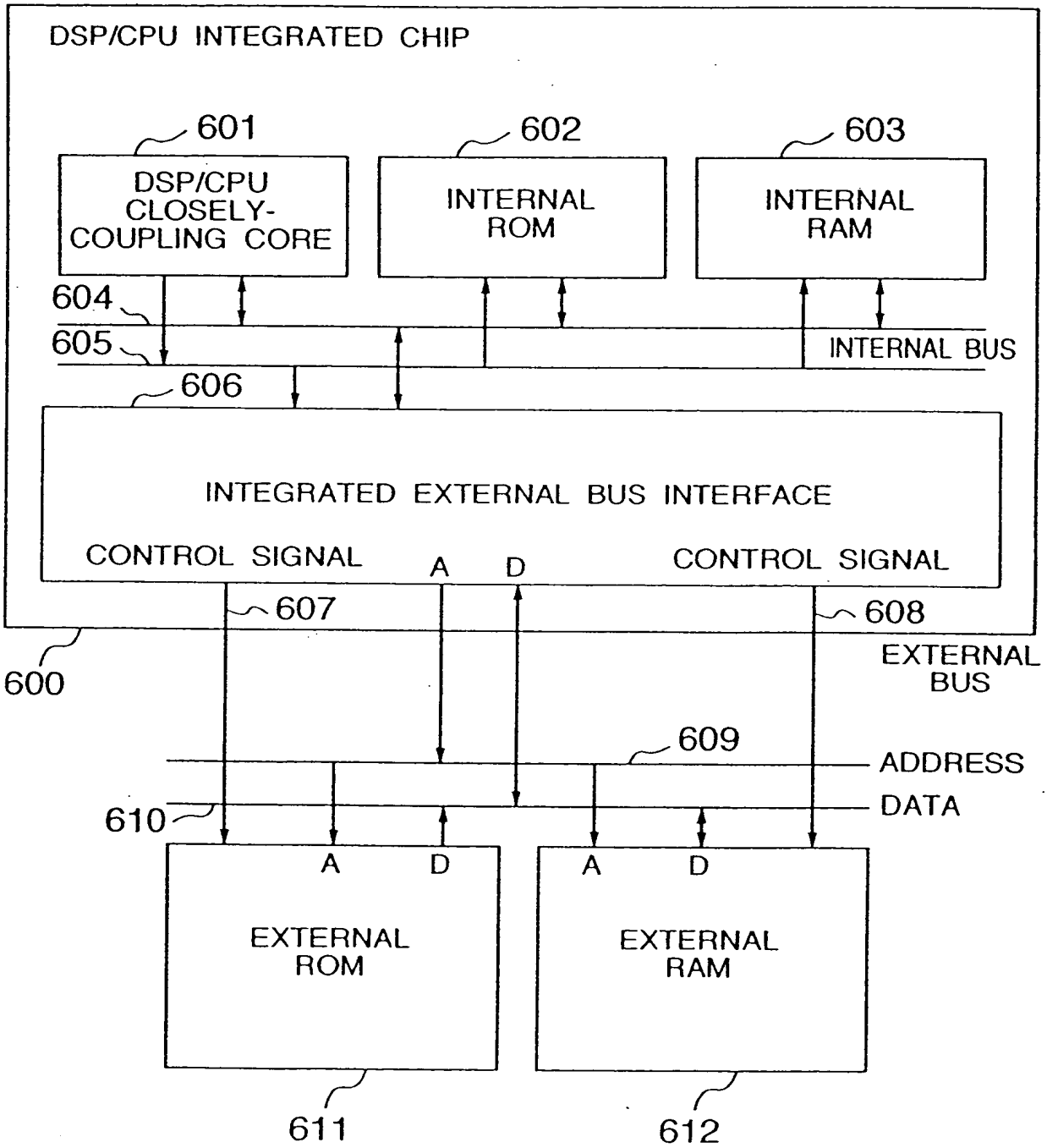

DSP/CPU INTEGRATED CHIP
601
602
603
DSP/CPU CLOSELY-COUPLING CORE
INTERNAL ROM
INTERNAL RAM
604
605
INTERNAL BUS
606
INTEGRATED EXTERNAL BUS INTERFACE
CONTROL SIGNAL
A
D
CONTROL SIGNAL
607
608
600
EXTERNAL BUS
609
ADDRESS
DATA
610
A
D
A
D
EXTERNAL ROM
EXTERNAL RAM
611
612

FIG. 7

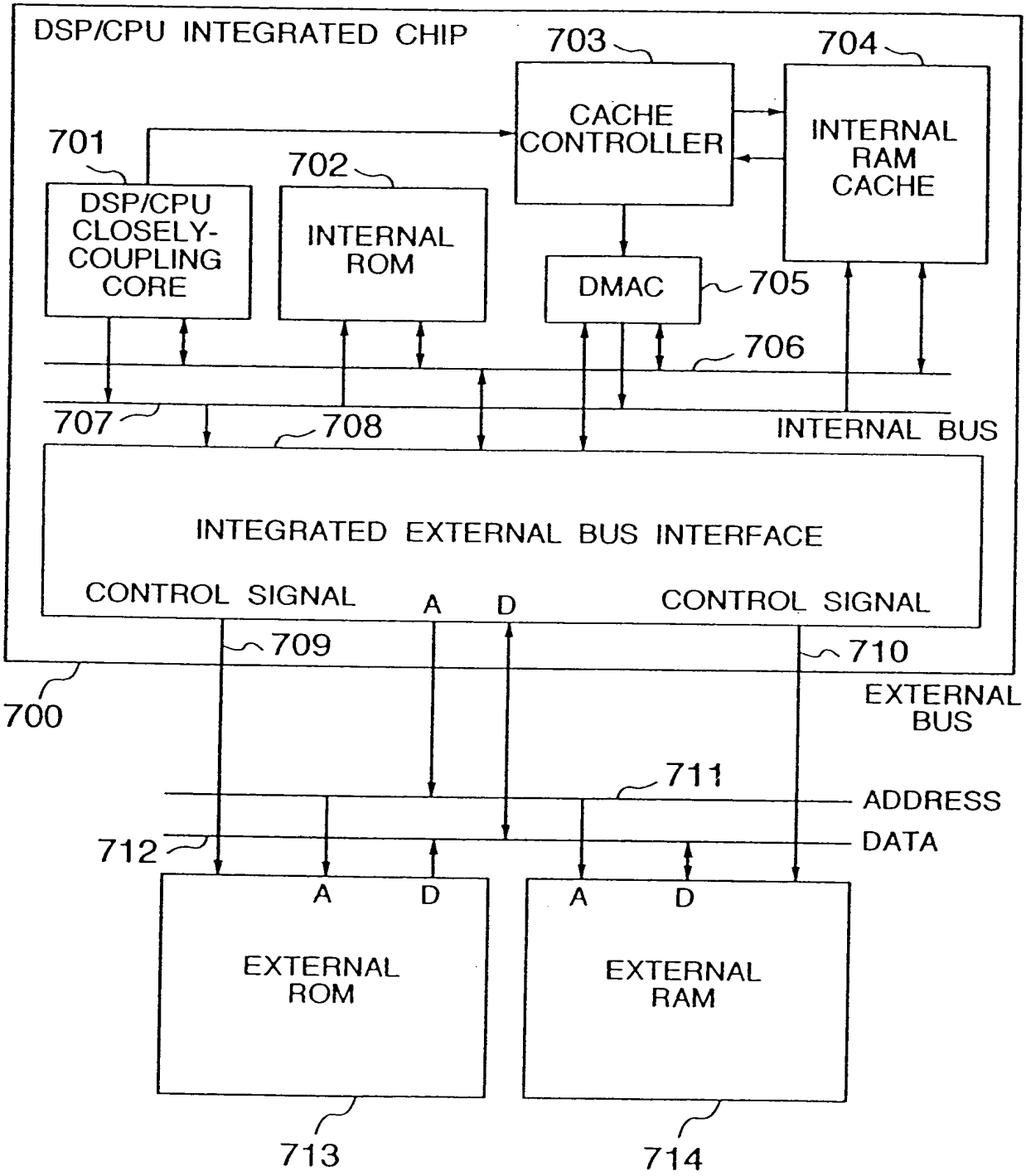

DSP/CPU INTEGRATED CHIP
703
704
CACHE CONTROLLER
INTERNAL RAM CACHE
701
702
DSP/CPU CLOSELY-COUPLING CORE
INTERNAL ROM
DMAC
705
706
707
708
INTERNAL BUS
INTEGRATED EXTERNAL BUS INTERFACE
CONTROL SIGNAL
A
D
CONTROL SIGNAL
709
710
700
EXTERNAL BUS
711
ADDRESS
712
DATA
A
D
A
D
EXTERNAL ROM
EXTERNAL RAM
713
714

FIG. 8

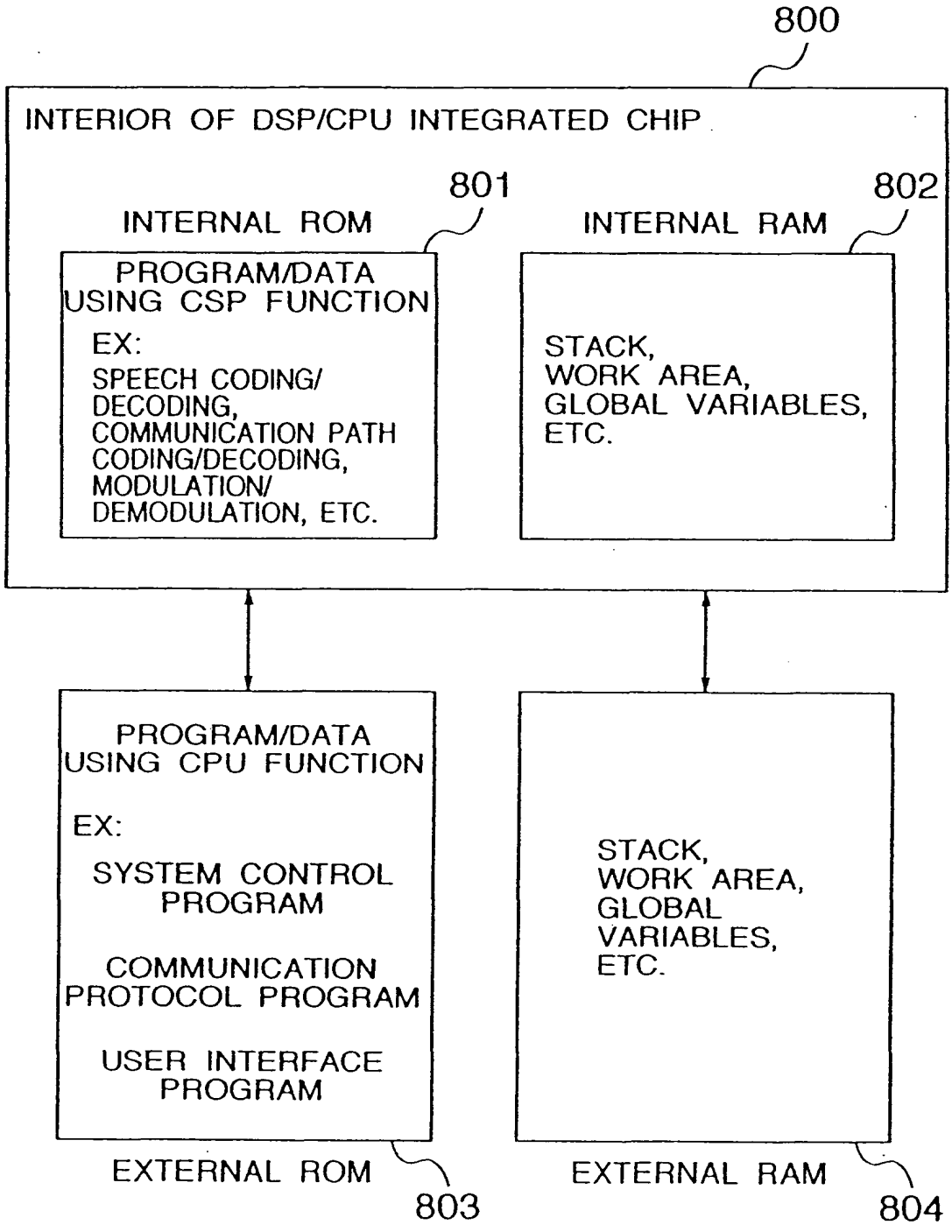

800
INTERIOR OF DSP/CPU INTEGRATED CHIP
801
INTERNAL ROM
802
INTERNAL RAM
PROGRAM/DATA USING CSP FUNCTION
EX:
SPEECH CODING/ DECODING, COMMUNICATION PATH CODING/DECODING, MODULATION/ DEMODULATION, ETC.
STACK, WORK AREA, GLOBAL VARIABLES, ETC.
PROGRAM/DATA USING CPU FUNCTION
EX:
SYSTEM CONTROL PROGRAM
COMMUNICATION PROTOCOL PROGRAM
USER INTERFACE PROGRAM
STACK, WORK AREA, GLOBAL VARIABLES, ETC.
EXTERNAL ROM
803
EXTERNAL RAM
804

FIG. 9

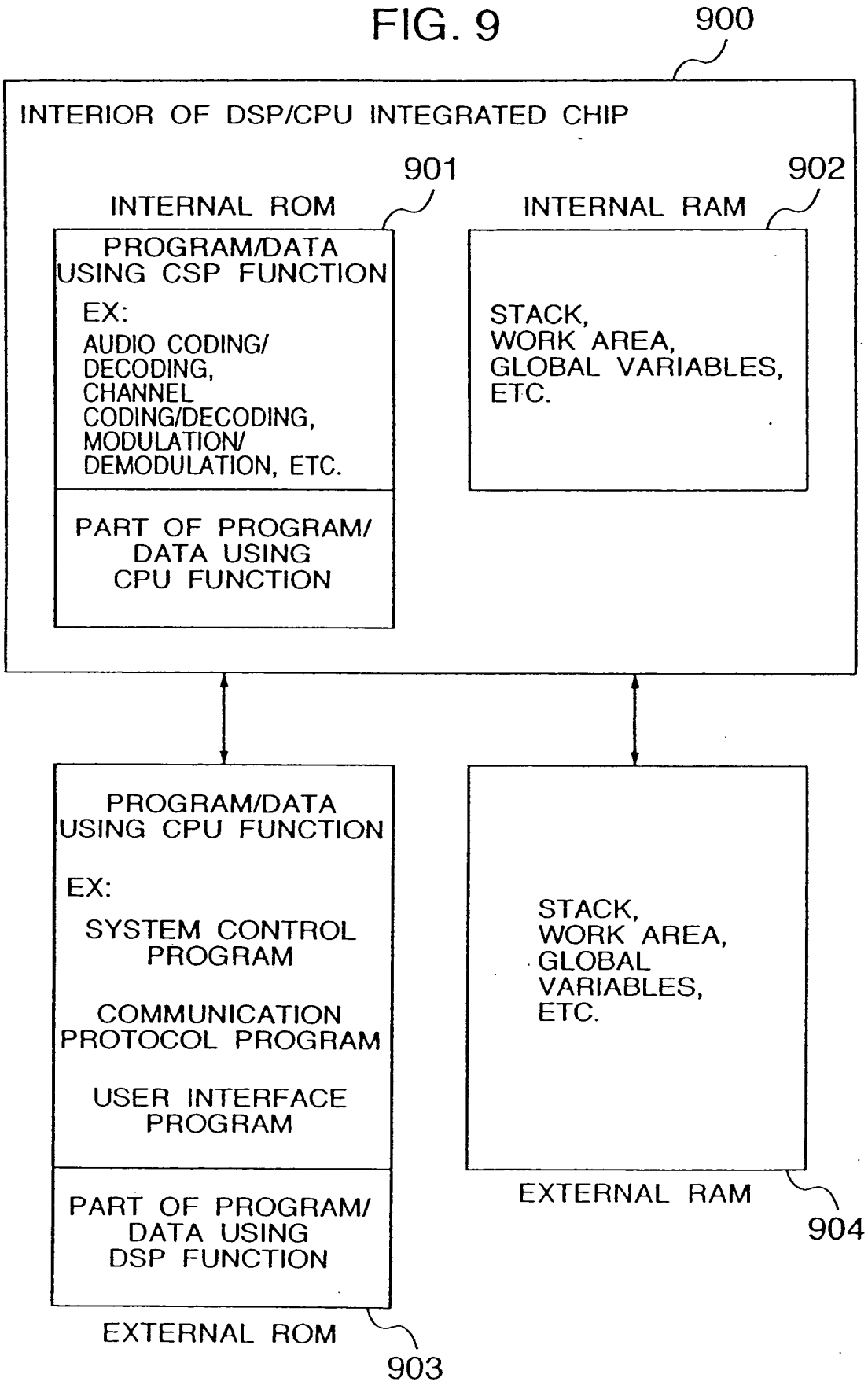

900
INTERIOR OF DSP/CPU INTEGRATED CHIP
901
INTERNAL ROM
902
INTERNAL RAM
PROGRAM/DATA USING CSP FUNCTION
EX:
AUDIO CODING/ DECODING, CHANNEL CODING/DECODING, MODULATION/ DEMODULATION, ETC.
PART OF PROGRAM/ DATA USING CPU FUNCTION
STACK, WORK AREA, GLOBAL VARIABLES, ETC.
PROGRAM/DATA USING CPU FUNCTION
EX:
SYSTEM CONTROL PROGRAM
COMMUNICATION PROTOCOL PROGRAM
USER INTERFACE PROGRAM
PART OF PROGRAM/ DATA USING DSP FUNCTION
EXTERNAL ROM
903
STACK, WORK AREA, GLOBAL VARIABLES, ETC.
EXTERNAL RAM
904

FIG. 10A

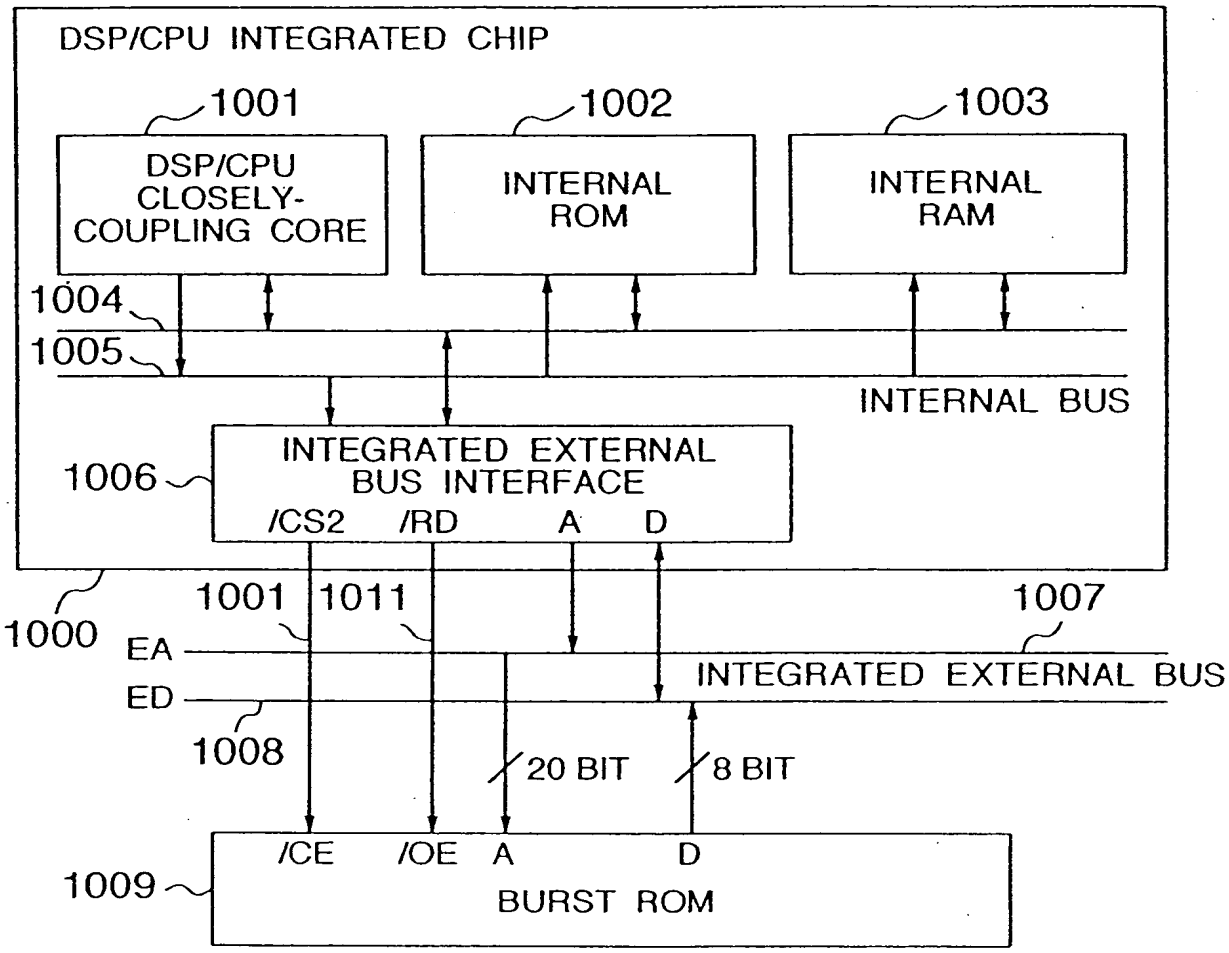


FIG. 10B

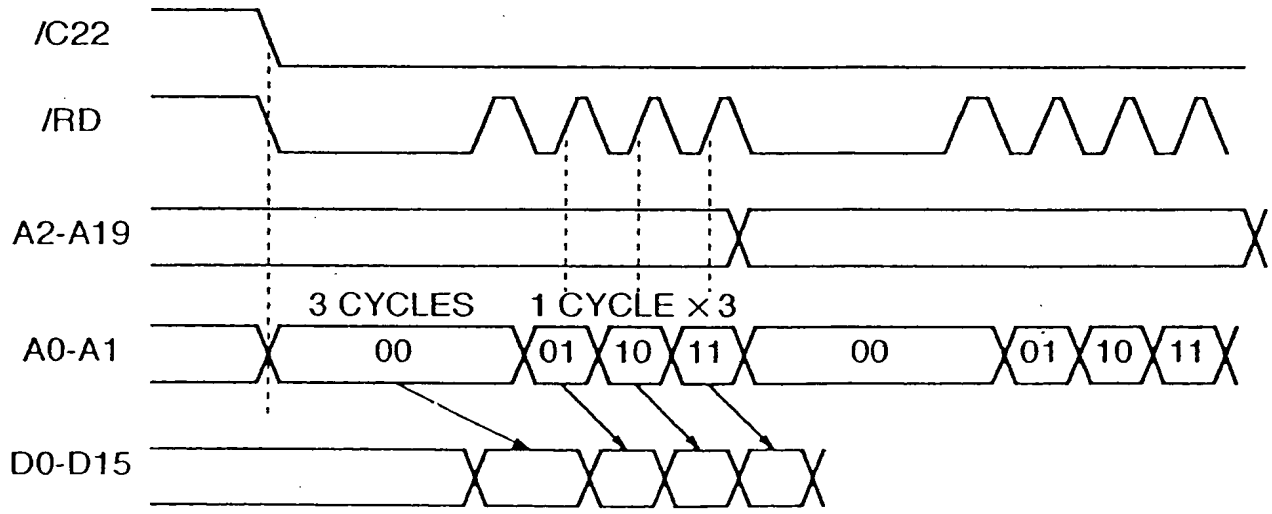


FIG. 11

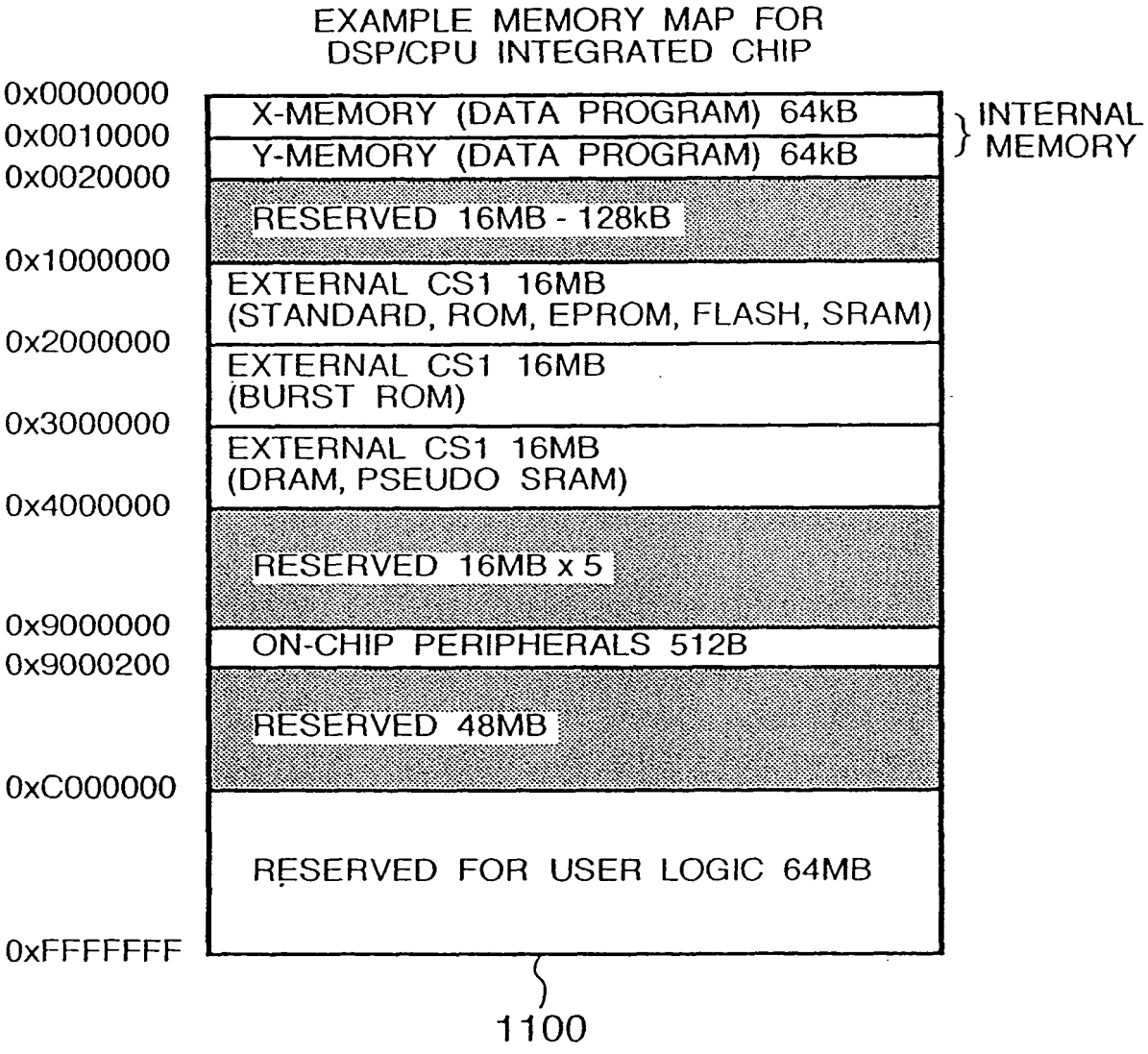

EXAMPLE MEMORY MAP FOR
DSP/CPU INTEGRATED CHIP
0x0000000
0x0010000
0x0020000
0x1000000
0x2000000
0x3000000
0x4000000
0x9000000
0x9000200
0xC000000
0xFFFFFFF
X-MEMORY (DATA PROGRAM) 64kB
Y-MEMORY (DATA PROGRAM) 64kB
INTERNAL MEMORY
RESERVED 16MB - 128kB
EXTERNAL CS1 16MB
(STANDARD, ROM, EPROM, FLASH, SRAM)
EXTERNAL CS1 16MB
(BURST ROM)
EXTERNAL CS1 16MB
(DRAM, PSEUDO SRAM)
RESERVED 16MB x 5
ON-CHIP PERIPHERALS 512B
RESERVED 48MB
RESERVED FOR USER LOGIC 64MB
1100

FIG. 12A

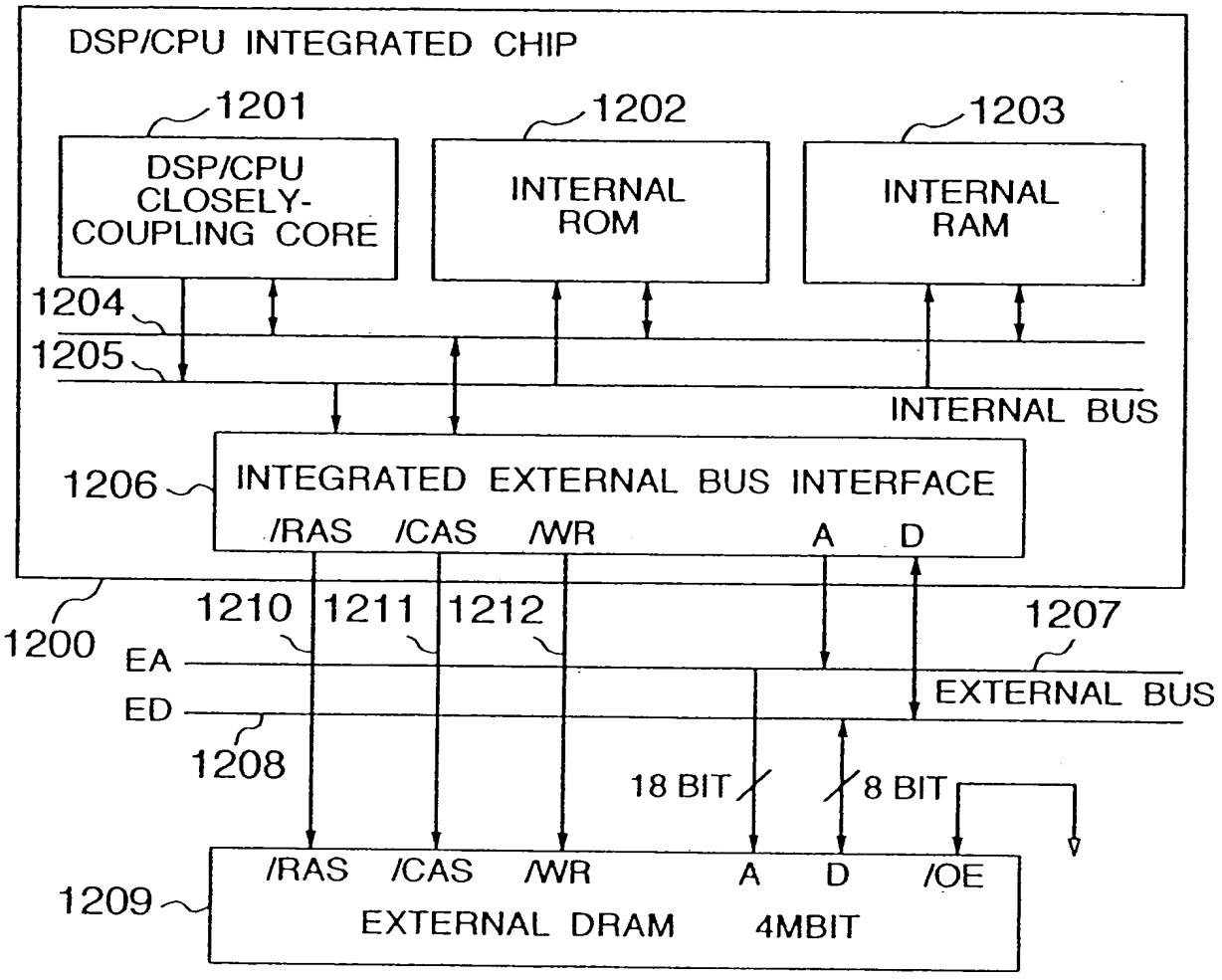


FIG. 12B

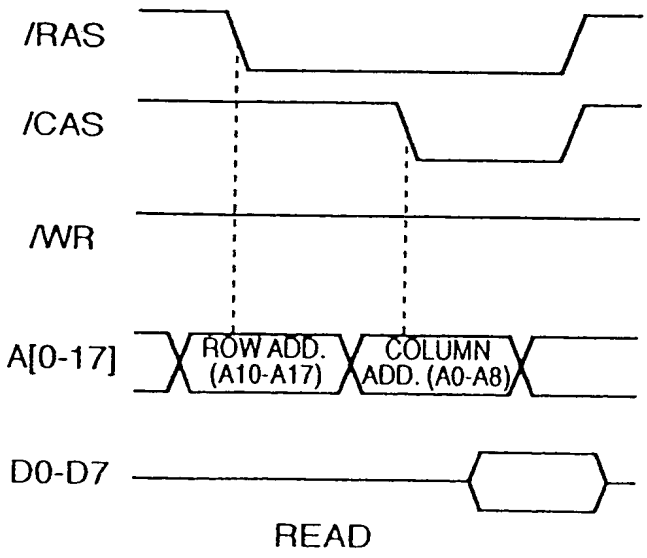


FIG. 12C

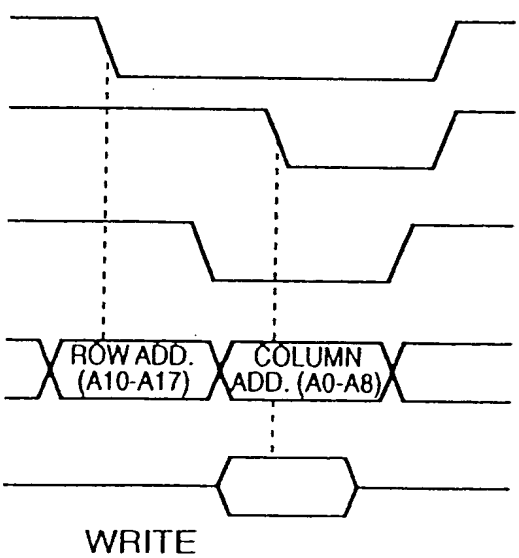


FIG. 13A

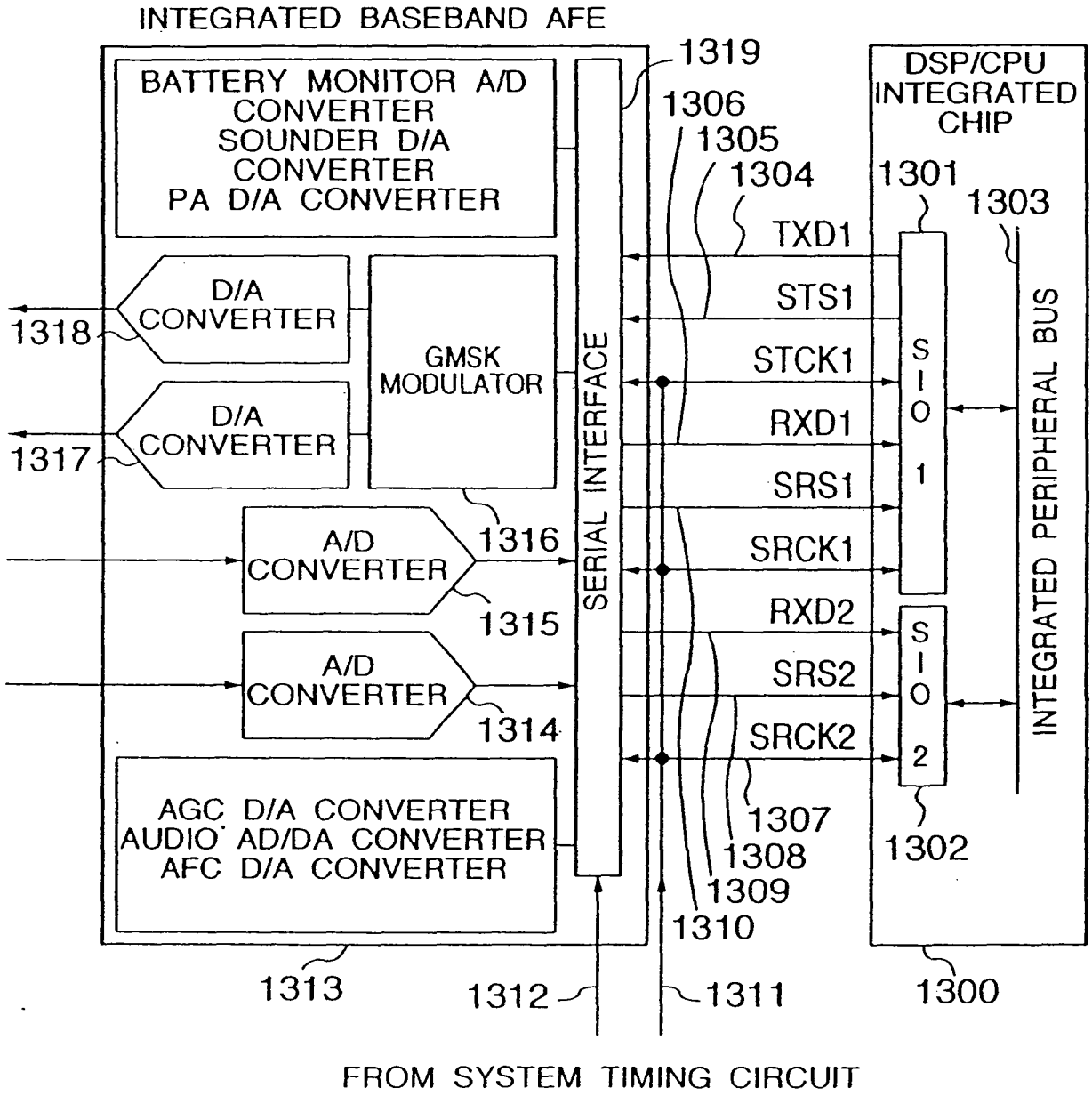

INTEGRATED BASEBAND AFE
BATTERY MONITOR A/D CONVERTER
SOUNDER D/A CONVERTER
PA D/A CONVERTER
D/A CONVERTER
1318
D/A CONVERTER
1317
GMSK MODULATOR
A/D CONVERTER
1316
1315
A/D CONVERTER
1314
AGC D/A CONVERTER
AUDIO AD/DA CONVERTER
AFC D/A CONVERTER
1313
SERIAL INTERFACE
1319
1306
1305
1304
TXD1
STS1
STCK1
RXD1
SRS1
SRCK1
RXD2
SRS2
SRCK2
1307
1308
1309
1310
1312
1311
DSP/CPU INTEGRATED CHIP
1301
1303
SIO1
SIO2
INTEGRATED PERIPHERAL BUS
1302
1300
FROM SYSTEM TIMING CIRCUIT

FIG. 13B

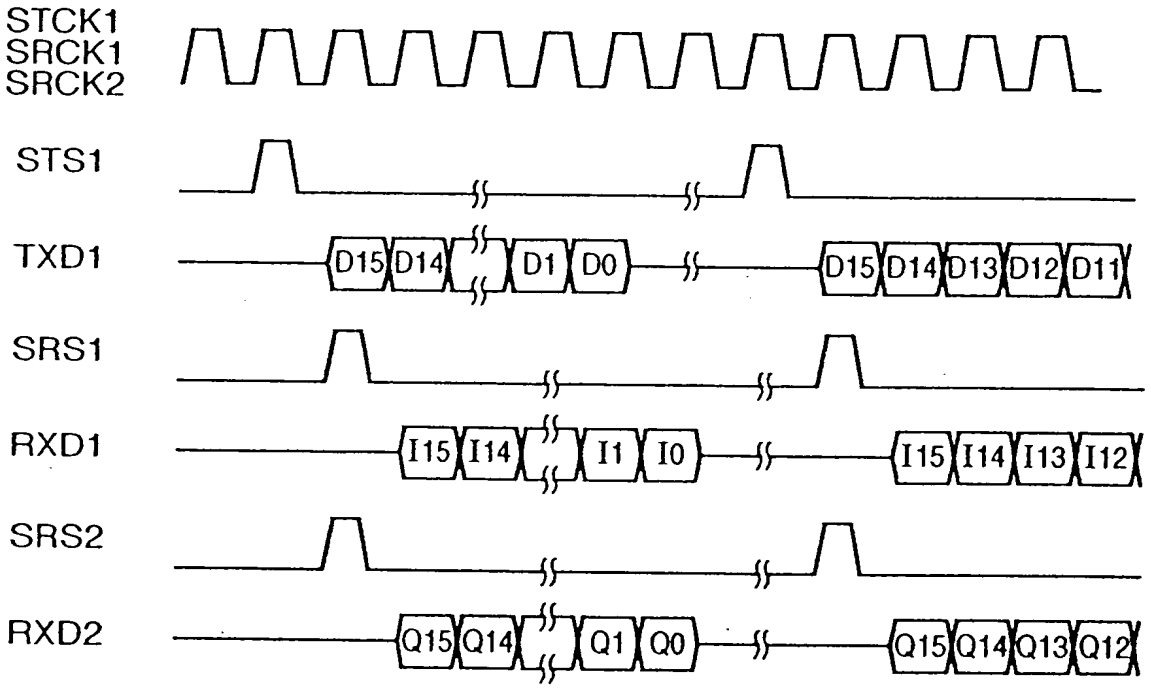

STCK1
SRCK1
SRCK2
STS1
TXD1
D15
D14
D1
D0
D15
D14
D13
D12
D11
SRS1
RXD1
I15
I14
I1
I0
I15
I14
I13
I12
SRS2
RXD2
Q15
Q14
Q1
Q0
Q15
Q14
Q13
Q12

FIG. 14

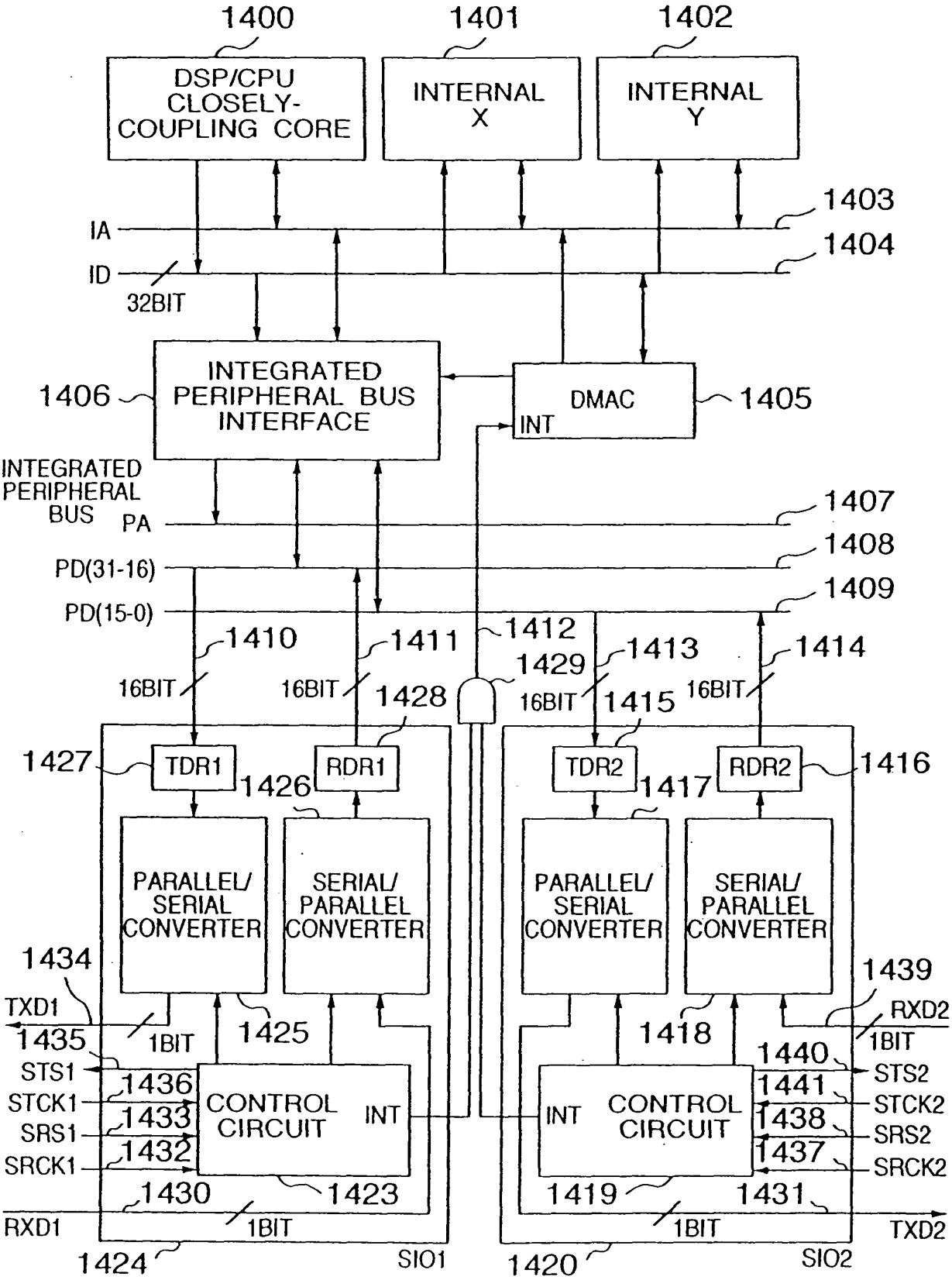

1400
1401
1402
DSP/CPU CLOSELY-COUPLING CORE
INTERNAL X
INTERNAL Y
1403
IA
1404
ID
32BIT
INTEGRATED PERIPHERAL BUS INTERFACE
1406
DMAC
INT
1405
INTEGRATED PERIPHERAL BUS
PA
1407
1408
PD(31-16)
1409
PD(15-0)
1410
1411
1412
1413
1414
16BIT
16BIT
1429
16BIT
1415
16BIT
1428
1427
TDR1
RDR1
1426
TDR2
1417
RDR2
1416
PARALLEL/ SERIAL CONVERTER
SERIAL/ PARALLEL CONVERTER
PARALLEL/ SERIAL CONVERTER
SERIAL/ PARALLEL CONVERTER
1434
1439
TXD1
RXD2
1435
1BIT
1425
1418
1BIT
1440
STS1
STS2
1436
1441
STCK1
CONTROL CIRCUIT
INT
STCK2
1433
1438
SRS1
INT
CONTROL CIRCUIT
SRS2
1432
1437
SRCK1
SRCK2
1430
1423
1419
1431
RXD1
1BIT
1BIT
TXD2
1424
SIO1
1420
SIO2

FIG. 15A

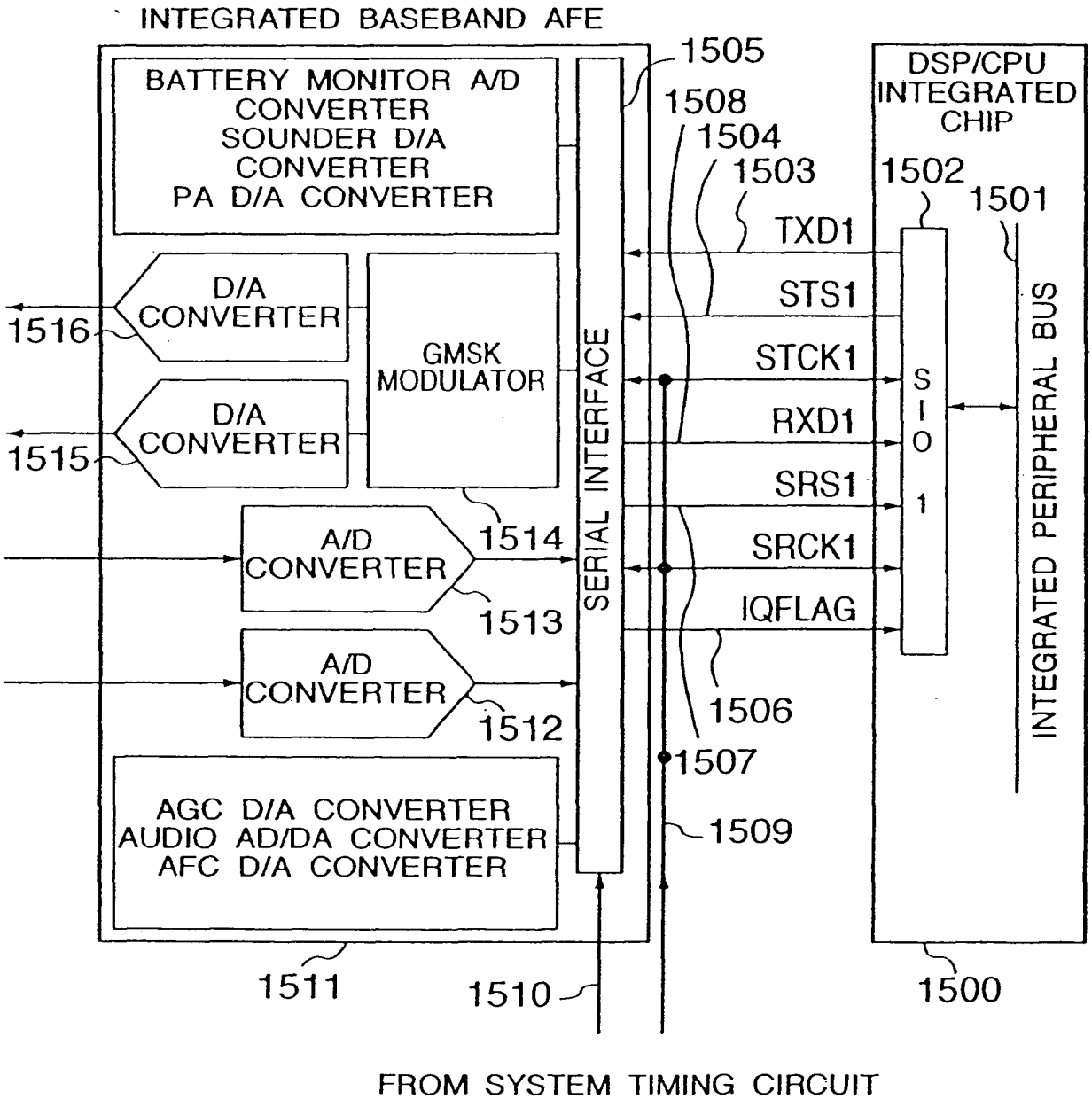

INTEGRATED BASEBAND AFE
BATTERY MONITOR A/D CONVERTER
SOUNDER D/A CONVERTER
PA D/A CONVERTER
D/A CONVERTER
D/A CONVERTER
GMSK MODULATOR
A/D CONVERTER
A/D CONVERTER
AGC D/A CONVERTER
AUDIO AD/DA CONVERTER
AFC D/A CONVERTER
SERIAL INTERFACE
1516
1515
1514
1513
1512
1511
1510
1505
1508
1504
1503
1502
1501
1506
1507
1509
1500
TXD1
STS1
STCK1
RXD1
SRS1
SRCK1
IQFLAG
S I O 1
DSP/CPU INTEGRATED CHIP
INTEGRATED PERIPHERAL BUS
FROM SYSTEM TIMING CIRCUIT

FIG. 15B

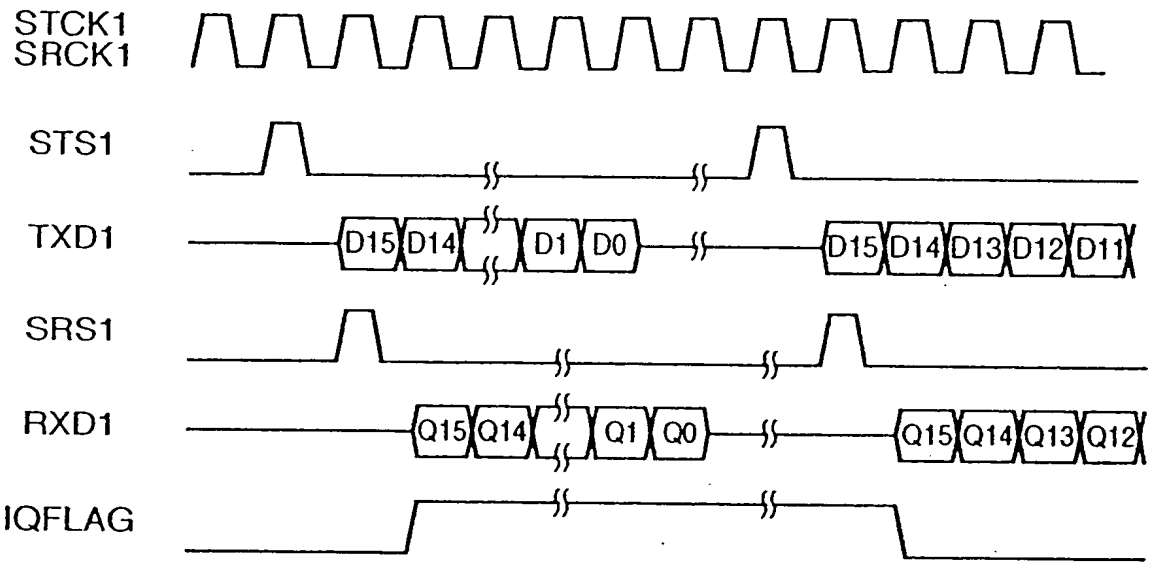

STCK1
SRCK1
STS1
TXD1
D15
D14
D1
D0
D15
D14
D13
D12
D11
SRS1
RXD1
Q15
Q14
Q1
Q0
Q15
Q14
Q13
Q12
IQFLAG

FIG. 16

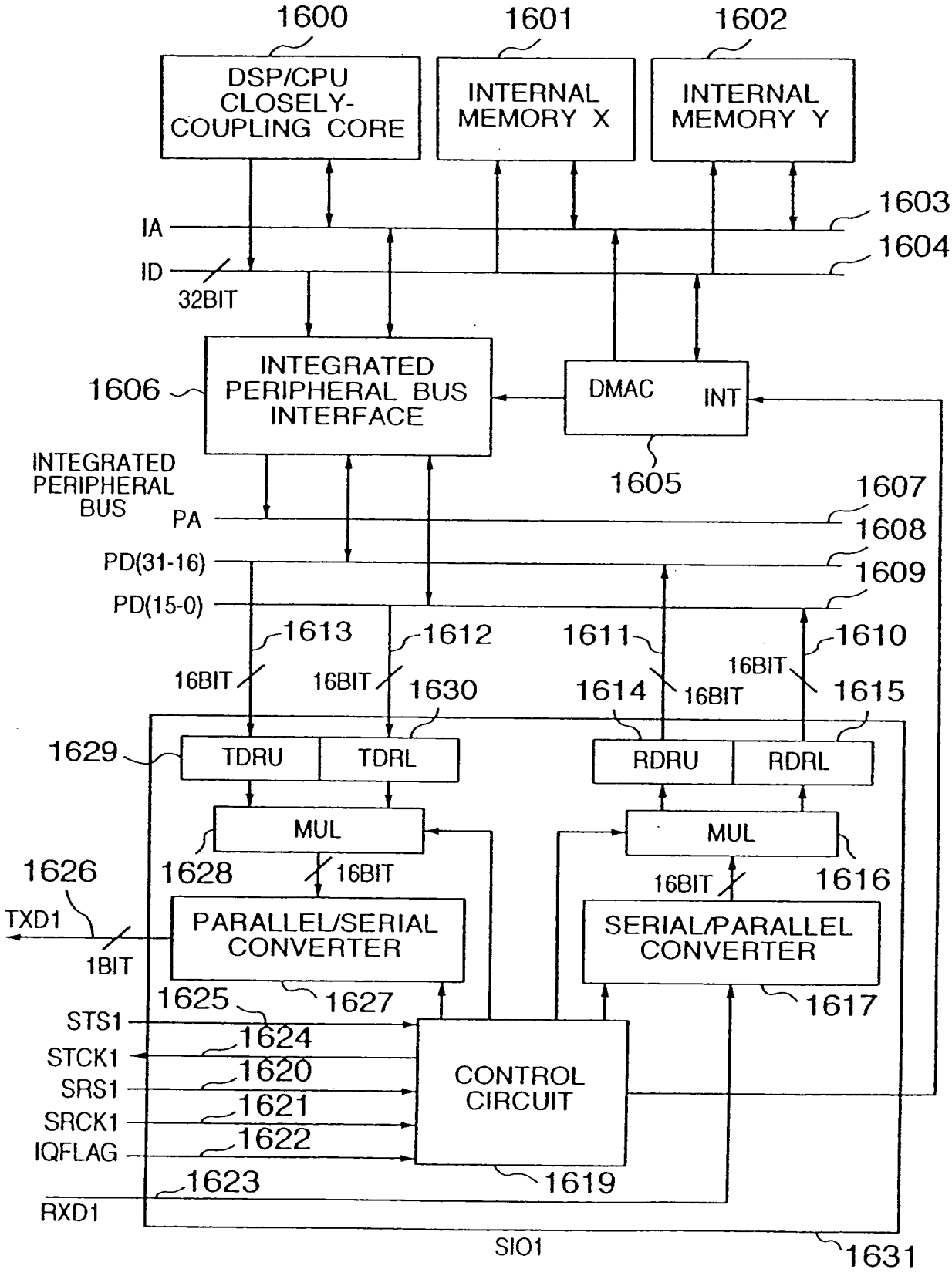
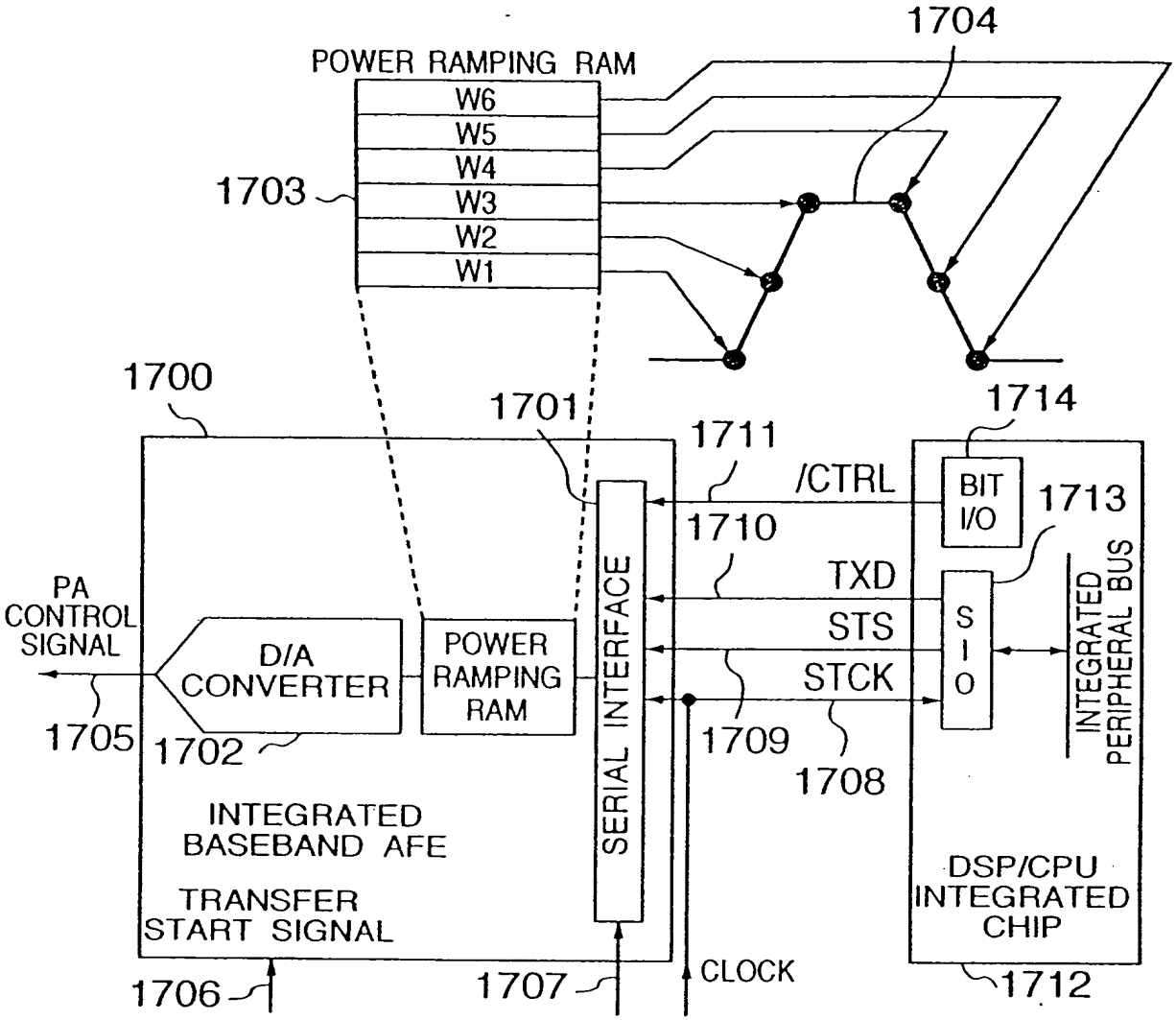
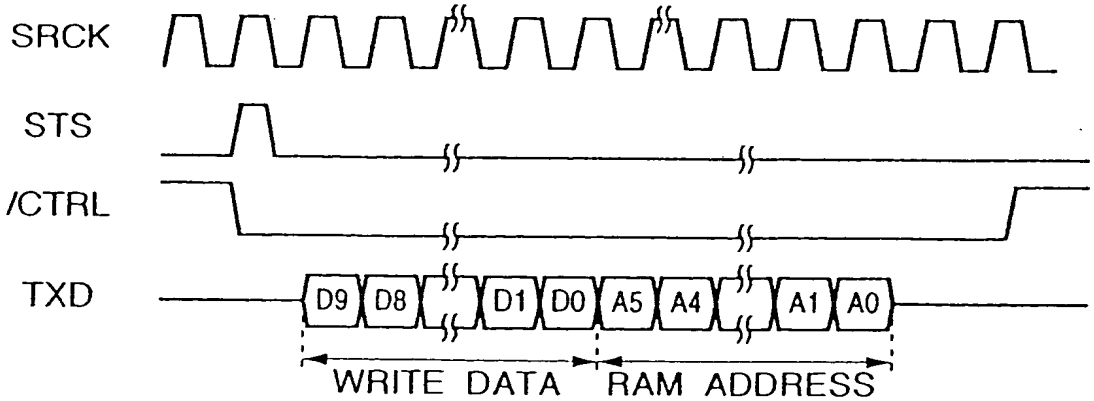

1600
1601
1602
DSP/CPU CLOSELY-COUPLING CORE
INTERNAL MEMORY X
INTERNAL MEMORY Y
1603
IA
1604
ID
32BIT
1606
INTEGRATED PERIPHERAL BUS INTERFACE
DMAC
INT
1605
INTEGRATED PERIPHERAL BUS
1607
PA
1608
PD(31-16)
1609
PD(15-0)
1613
1612
1611
1610
16BIT
16BIT
1630
1614
16BIT
16BIT
1615
1629
TDRU
TDRL
RDRU
RDRL
MUL
MUL
1626
1628
16BIT
16BIT
1616
TXD1
PARALLEL/SERIAL CONVERTER
SERIAL/PARALLEL CONVERTER
1BIT
1627
1617
1625
STS1
1624
STCK1
1620
SRS1
1621
SRCK1
1622
IQFLAG
CONTROL CIRCUIT
1623
1619
RXD1
SIO1
1631

FIG. 17A



FROM SYSTEM TIMING CIRCUIT

FIG. 17B



WRITE TIMING OF POWER RAMPING RAM

FIG. 18

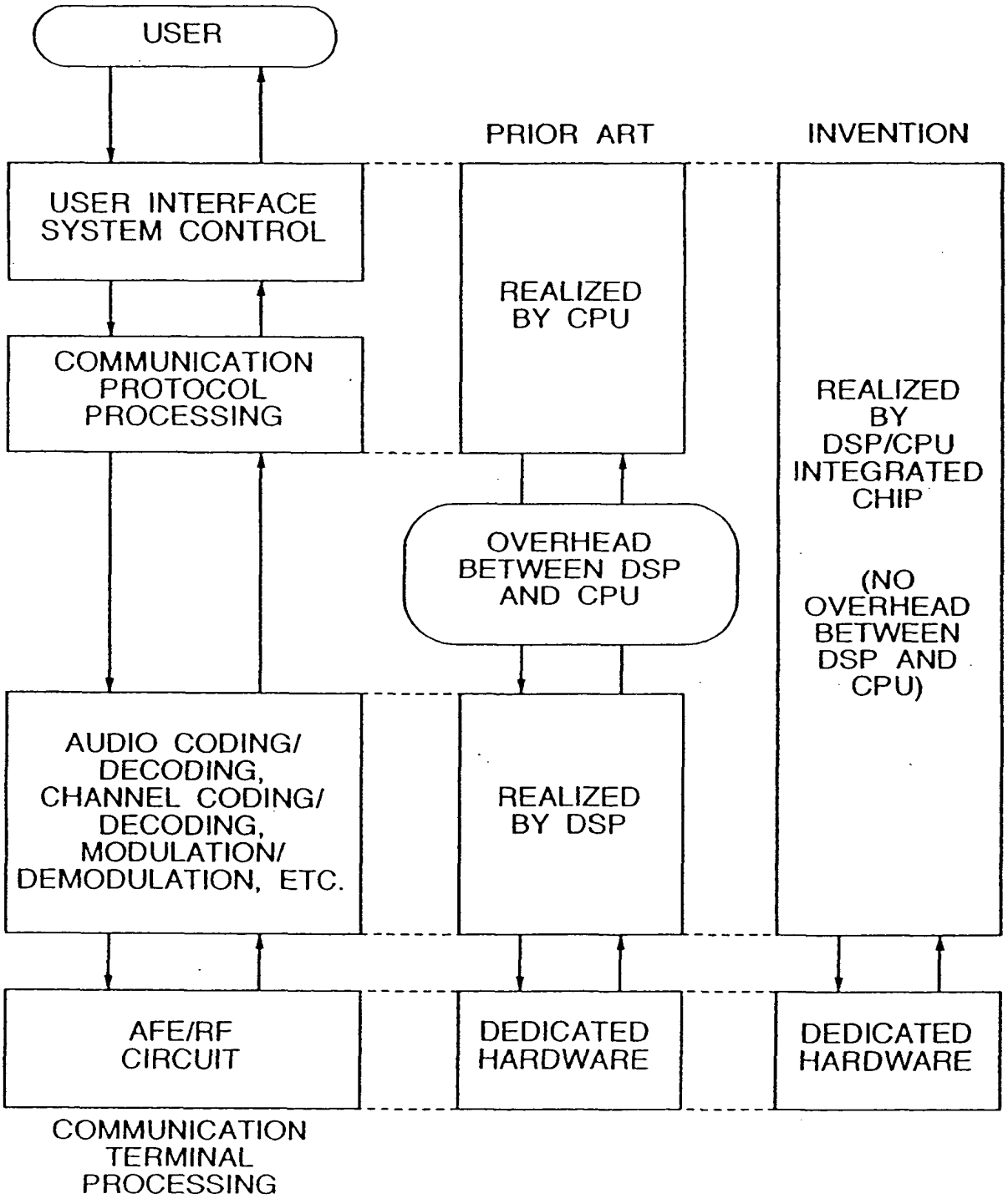

USER
PRIOR ART
INVENTION
USER INTERFACE SYSTEM CONTROL
COMMUNICATION PROTOCOL PROCESSING
REALIZED BY CPU
REALIZED BY DSP/CPU INTEGRATED CHIP
(NO OVERHEAD BETWEEN DSP AND CPU)
OVERHEAD BETWEEN DSP AND CPU
AUDIO CODING/ DECODING, CHANNEL CODING/ DECODING, MODULATION/ DEMODULATION, ETC.
REALIZED BY DSP
AFE/RF CIRCUIT
DEDICATED HARDWARE
DEDICATED HARDWARE
COMMUNICATION TERMINAL PROCESSING

FIG. 19

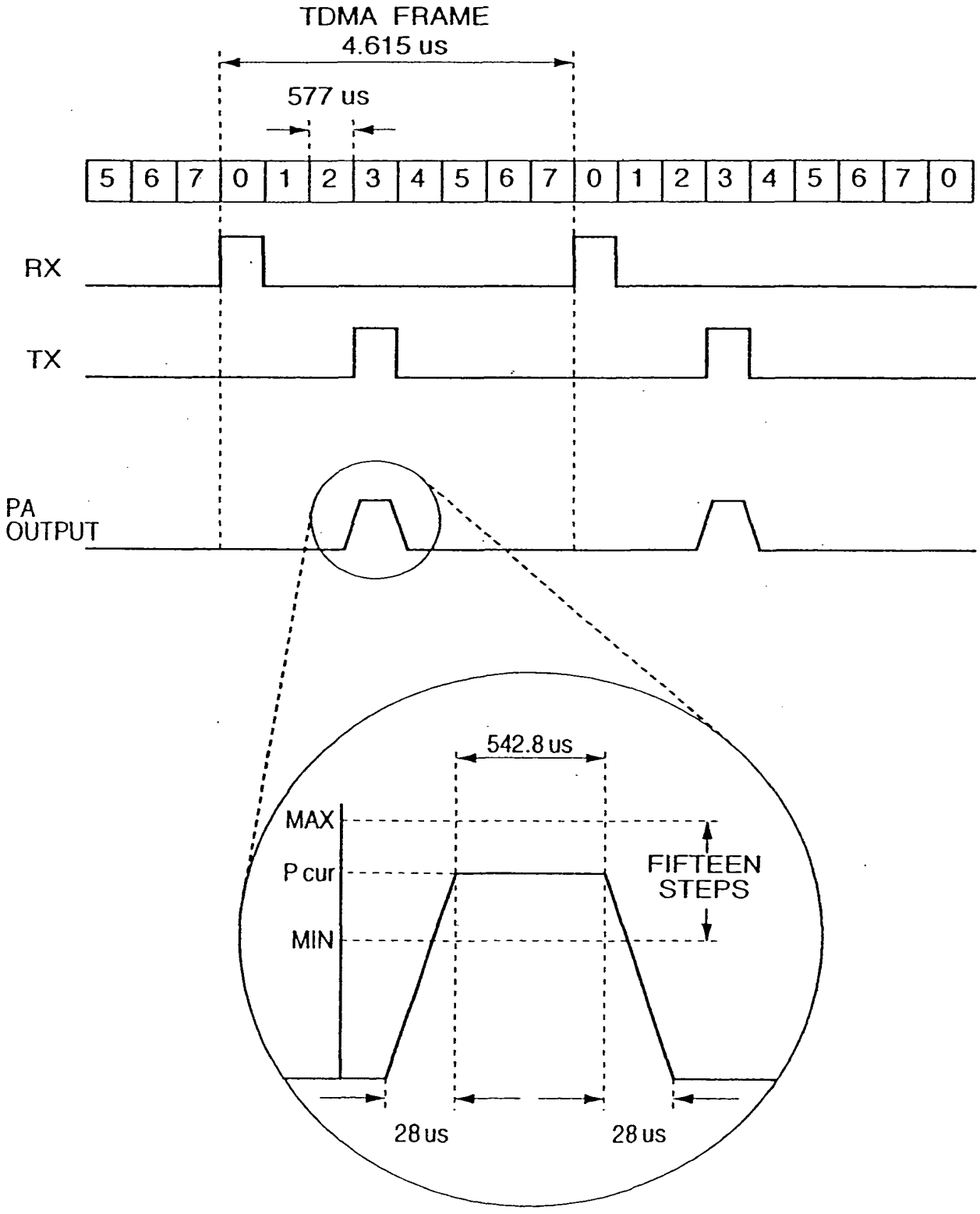

TDMA FRAME
4.615 us
577 us
5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0
RX
TX
PA
OUTPUT
542.8 us
MAX
P cur
MIN
FIFTEEN
STEPS
28 us
28 us

FIG. 20A

PRIOR ART

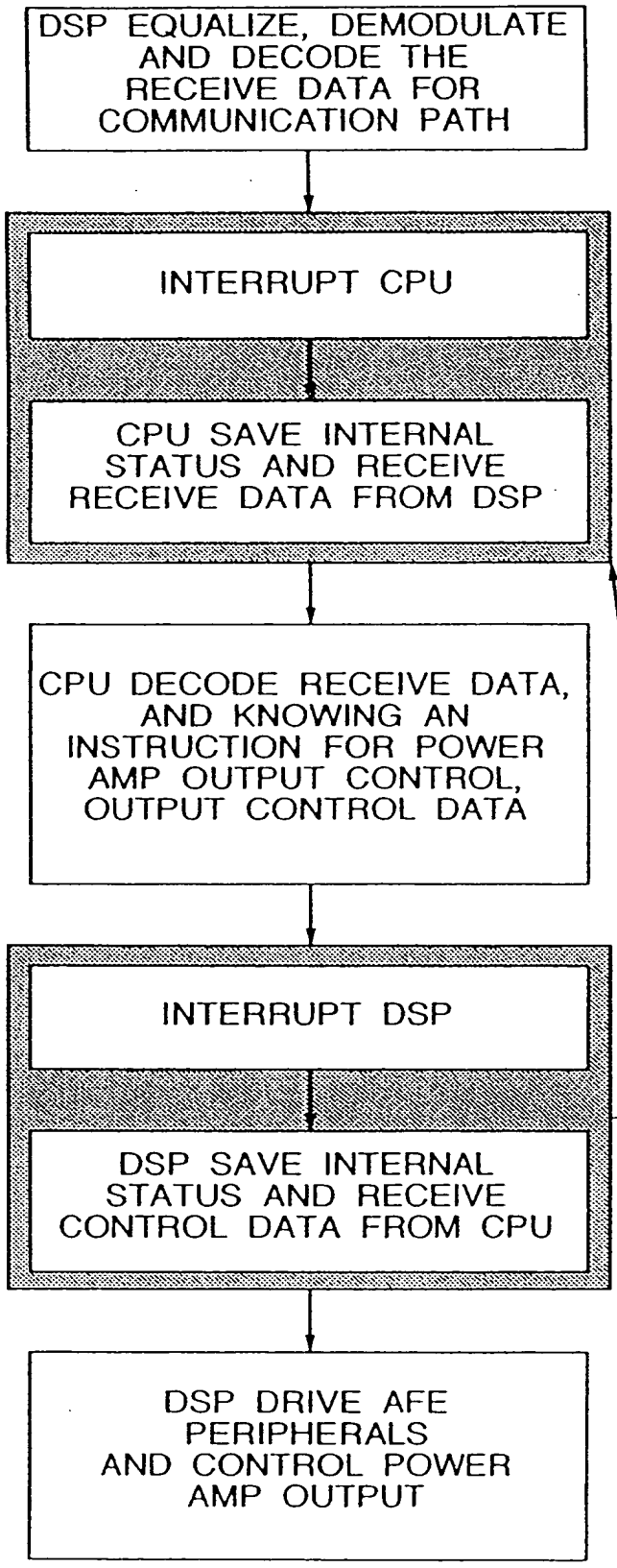


FIG. 20B

INVENTION

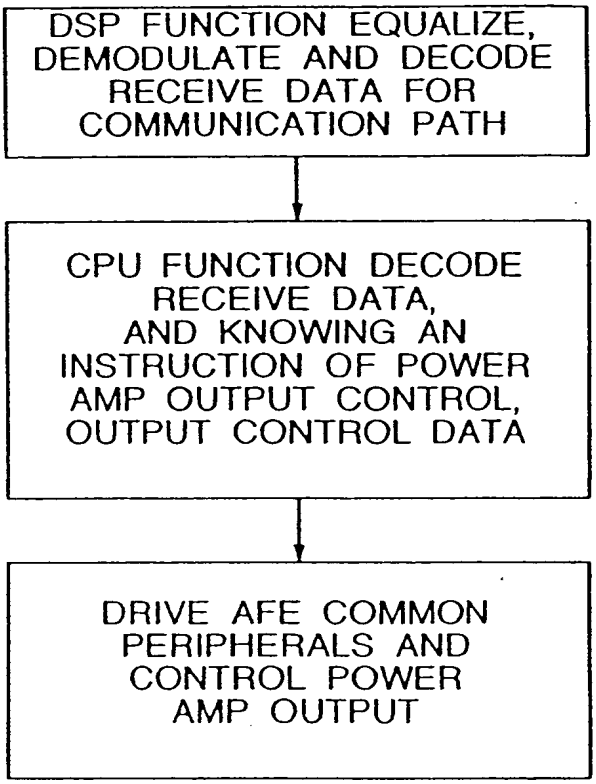


FIG. 21

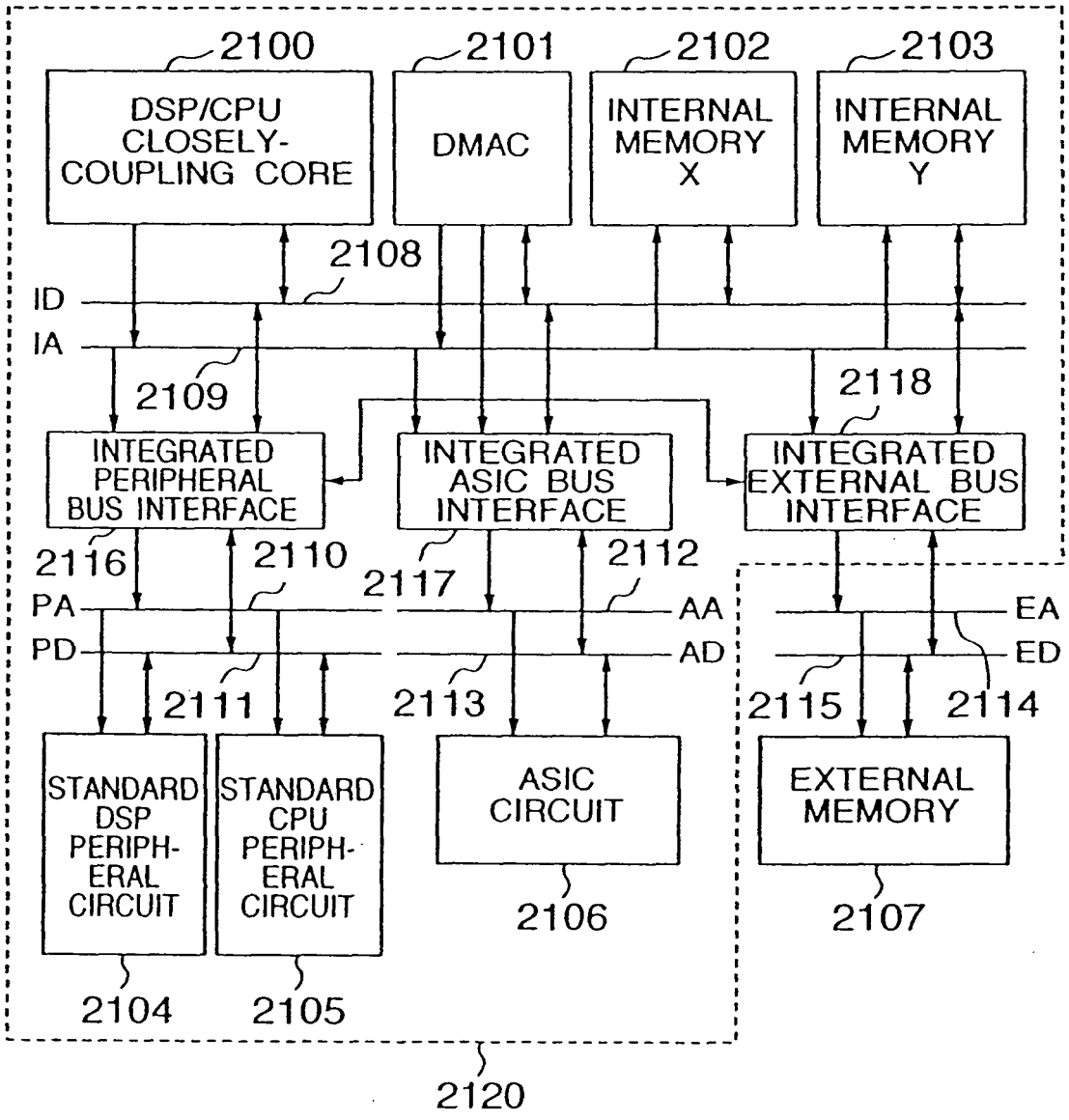

2100
2101
2102
2103
DSP/CPU CLOSELY-COUPLING CORE
DMAC
INTERNAL MEMORY X
INTERNAL MEMORY Y
2108
ID
IA
2109
2118
INTEGRATED PERIPHERAL BUS INTERFACE
INTEGRATED ASIC BUS INTERFACE
INTEGRATED EXTERNAL BUS INTERFACE
2116
2110
2117
2112
PA
PD
AA
AD
EA
ED
2111
2113
2115
2114
STANDARD DSP PERIPH-ERAL CIRCUIT
STANDARD CPU PERIPH-ERAL CIRCUIT
ASIC CIRCUIT
EXTERNAL MEMORY
2104
2105
2106
2107
2120

FIG. 22

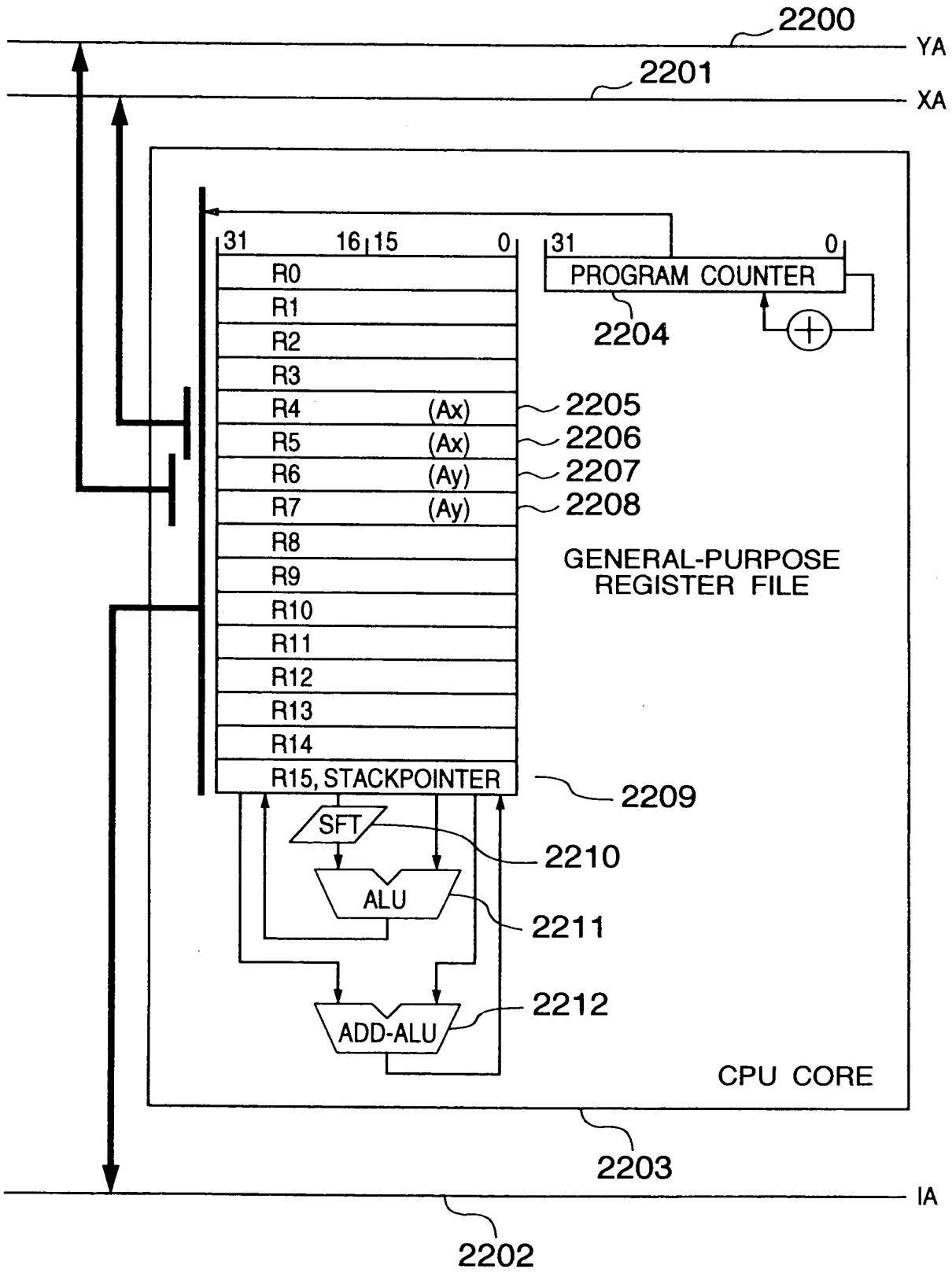

2200
YA
2201
XA
31
16
15
0
R0
R1
R2
R3
R4 (Ax)
R5 (Ax)
R6 (Ay)
R7 (Ay)
R8
R9
R10
R11
R12
R13
R14
R15, STACKPOINTER
2205
2206
2207
2208
GENERAL-PURPOSE REGISTER FILE
31
0
PROGRAM COUNTER
2204
2209
SFT
2210
ALU
2211
ADD-ALU
2212
CPU CORE
2203
IA
2202

FIG. 23

```
short  XARRAY[4]={1,2,3,4};
short  YARRAY[4]={1,1,1,1};
short  ZARRAY[2];

main(){

        short  *x_pntr, *y_pntr1, *y_pntr2;

        x_pntr=XARRAY;      /*INITIALING x_pntr*/
        y_pntr1=YARRAY;     /*INITIALING y_pntr1*/
        y_pntr=ZARRAY;      /*INITIALING y_pntr2*/

        /*CALL MULTIPLY AND ACCUMULATE ROUTINE/*
        mac_sss(4, x_pntr, y_pntr1, y_pntr2);
}
```

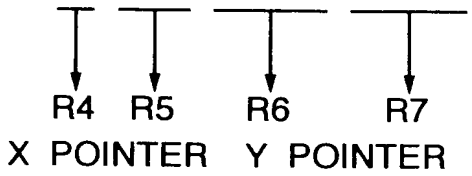
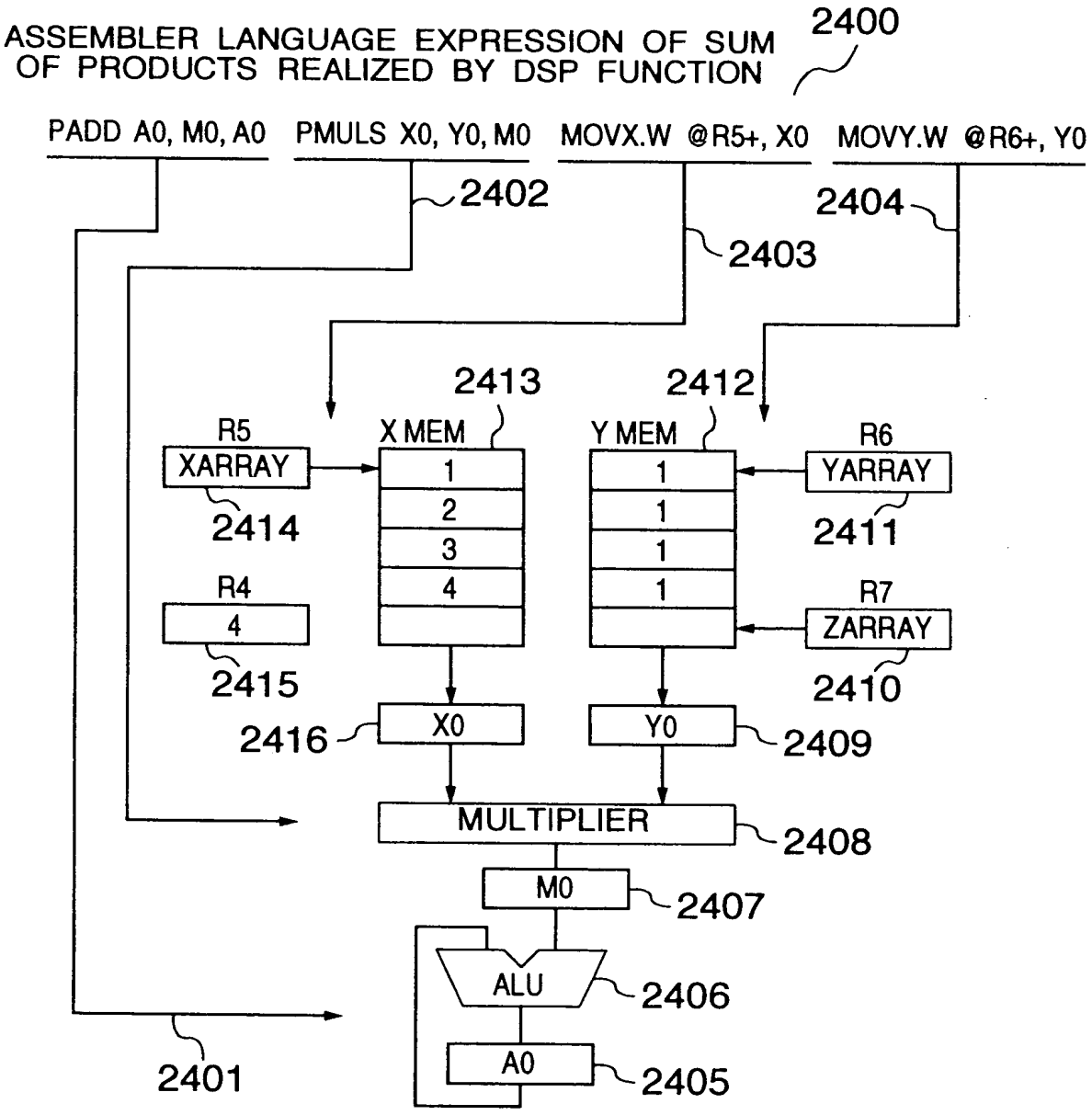


FIG. 24


ASSEMBLER LANGUAGE EXPRESSION OF SUM OF PRODUCTS REALIZED BY DSP FUNCTION
2400
PADD A0, M0, A0
PMULS X0, Y0, M0
MOVX.W @R5+, X0
MOVY.W @R6+, Y0
2402
2403
2404
2413
2412
R5
XARRAY
2414
X MEM
1
2
3
4
Y MEM
1
1
1
1
R6
YARRAY
2411
R4
4
2415
R7
ZARRAY
2410
2416
X0
Y0
2409
MULTIPLIER
2408
M0
2407
ALU
2406
A0
2405
2401